

# HELLCAT 13" Schematics

## Comet Lake-U

2019-10-27

REV : DVT1

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*DY : None Installed*

*UMA: UMA only installed*

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A3

Document Number

**JEDI 13"**

Rev

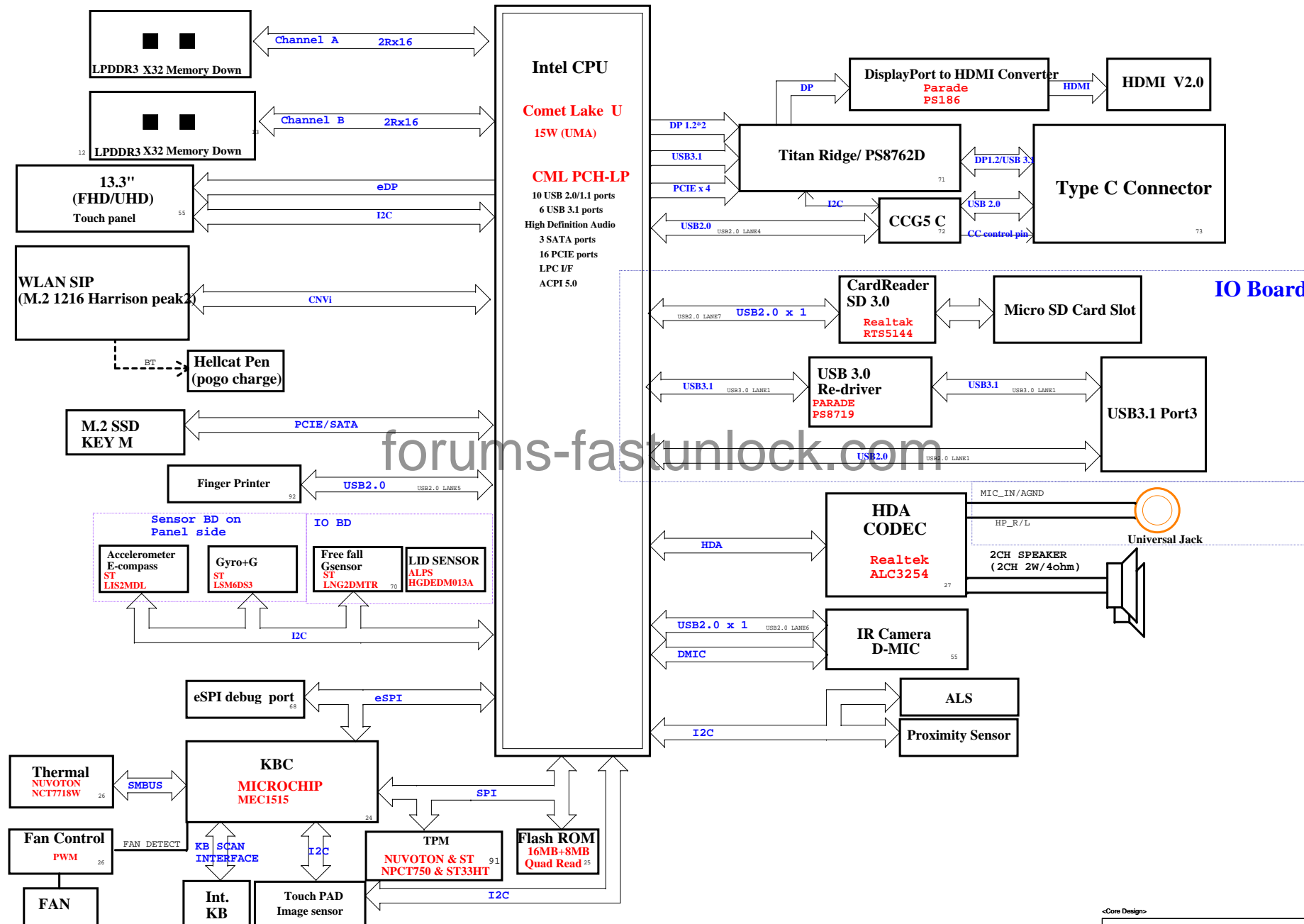
**SC**

Date: Monday, October 28, 2019

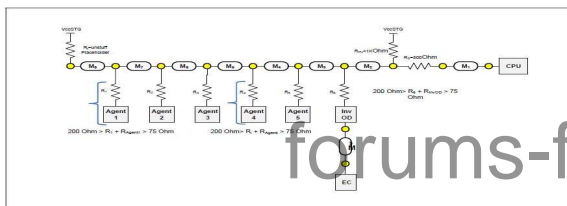
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# CML-U 13" CPU 15W Block Diagram

Project code:  
PCB P/N: 19721  
Revision: SA



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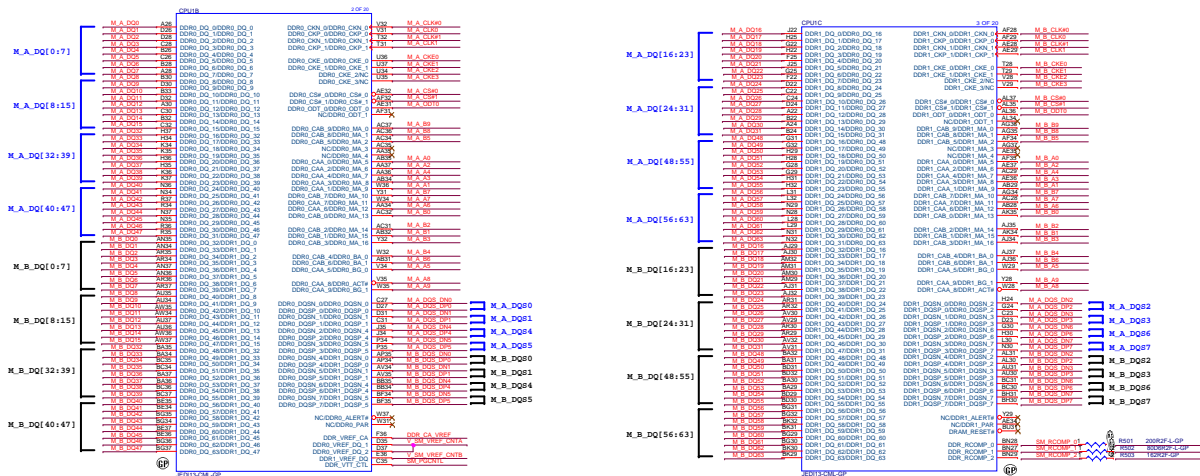
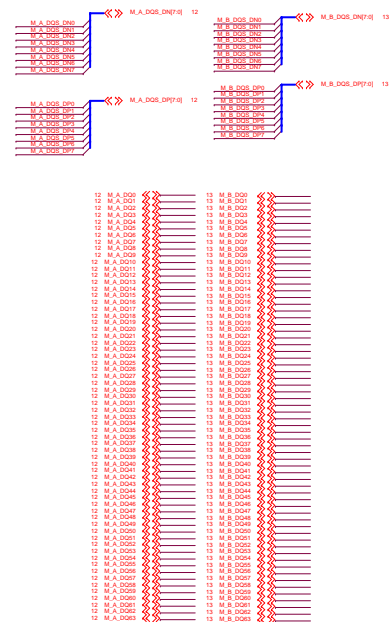


**Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)**

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
<b>Topology Guidelines</b>							
Platform resistors values		Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω					
Platform resistors tolerances		± 5%					

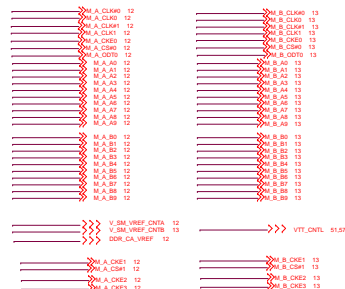
Date: Monday, October 28, 2019 Sheet 4 of 106

## DDR4 ball type: Non-Interleaved Type



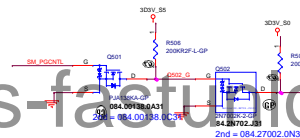
Signal Name	Value	Length
RCCOMP[0]	200R_14	Max = 500 mils
RCCOMP[1]	80_6R_14	Max = 500 mils
RCCOMP[2]	162R_14	Max = 500 mils

Layout Note:  
SM\_RCOMP keep routing length less than 500 mils.

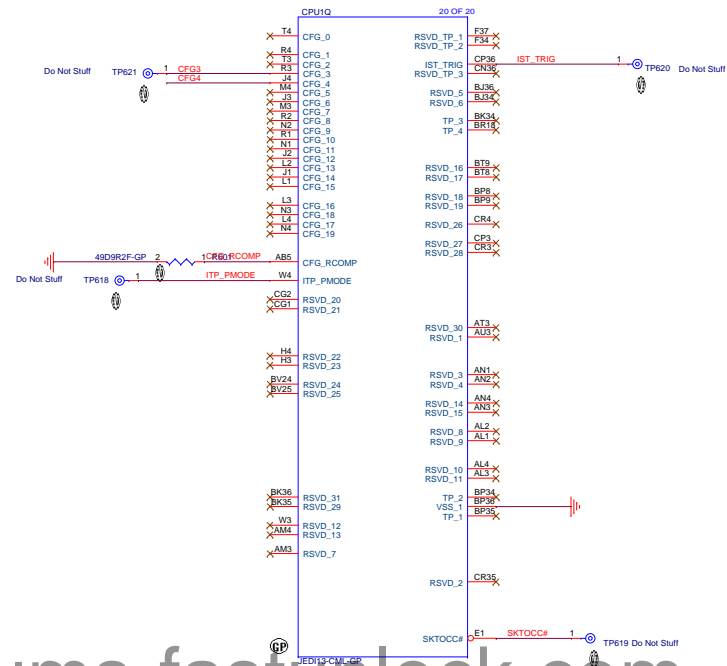


DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.  
Clock (CLK and CLKB) and Strobe (DSQ and DQSB) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

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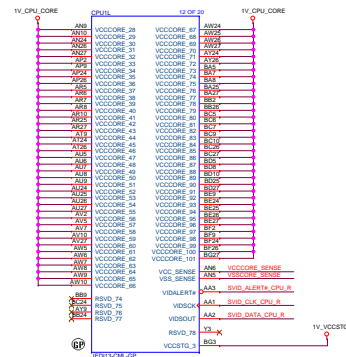


15 CFG3 <<>>  
15 CFG4 <<>>



46 VCCORE\_SENSE#  
46 VCCORE\_SENSE#

46 SVID\_DATA\_CPU  
46 SVID\_CLK\_CPU  
46 SVID\_ALERT#\_CPU

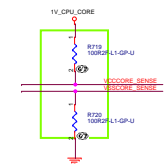
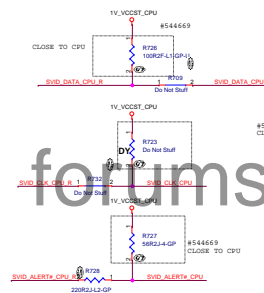


Layout Note:  
The total length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).  
Route the Alert signal between the Clock and the Data signals.

SVID DATA

SVID CLOCK

SVID ALERT



Layout Note:  
1. Place close to CPU  
2. VCCORE\_SENSE/ VCCORE\_SENSE impedance=50 ohm  
3. Length match=294.1

Figure 7-19. Routing Illustration for SVID Topology

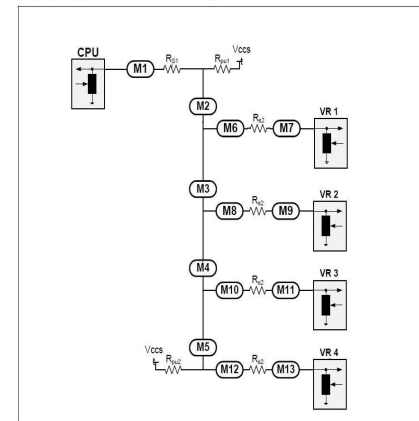


Table 7-18. SVID# Routing Guidelines (Sheet 2 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381		15000	
M3	MS/SL/DSL	VSS		102	432	4015.75	17007.9
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11

Topology Guidelines	
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=100Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock
Length Matching Rules	
Length Matching between VIDSOUT and VIDSCK	± 100mils






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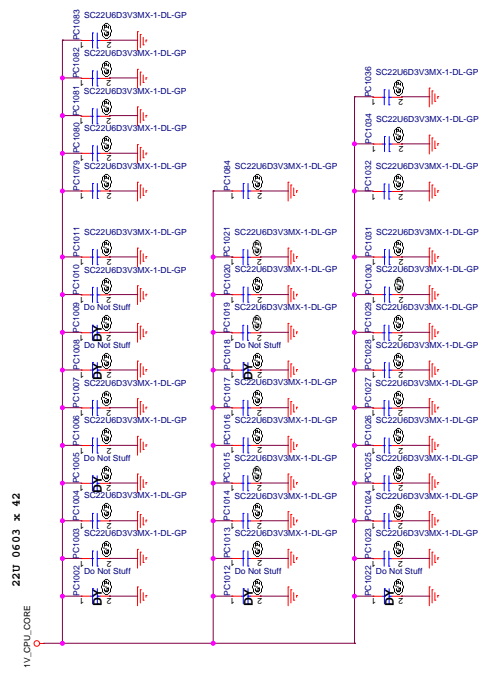
Rev  
SC

Date: Monday, October 28, 2019

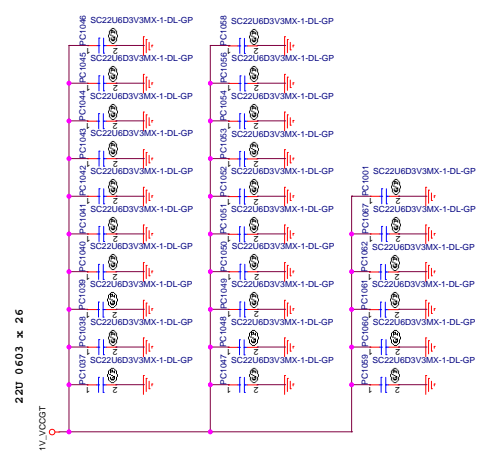
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Main Func = CPU

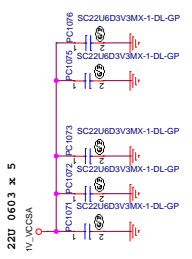
# 1V\_CPU\_CORE



# VCCGT



# VCCSA



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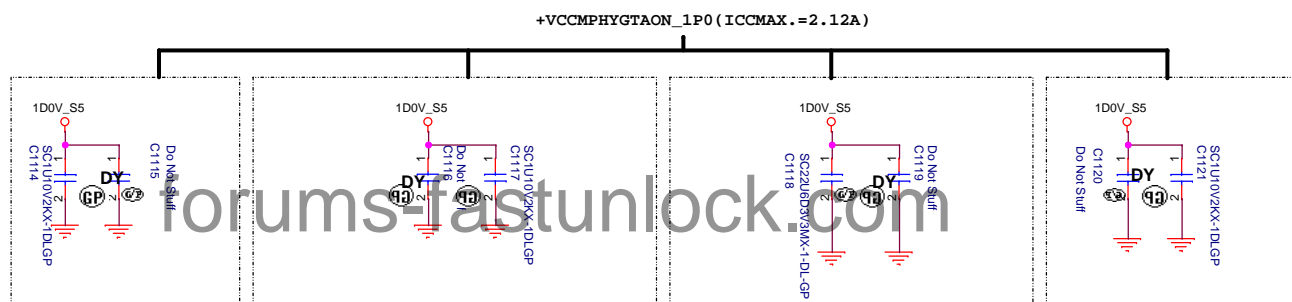
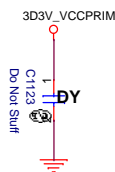
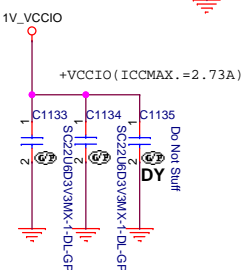
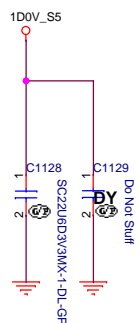
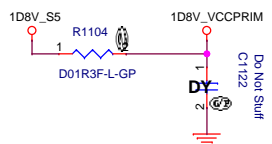
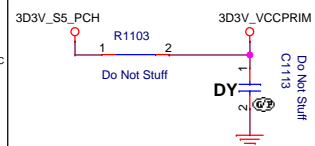
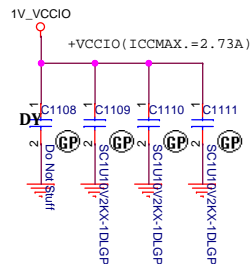
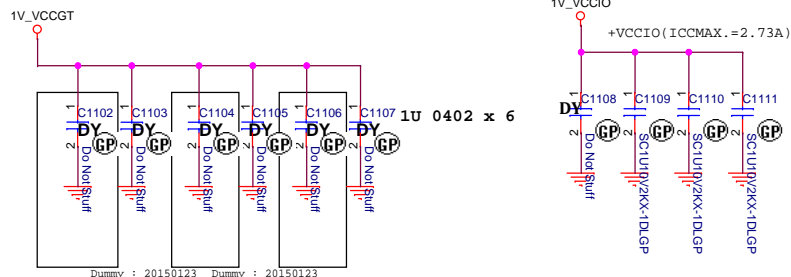
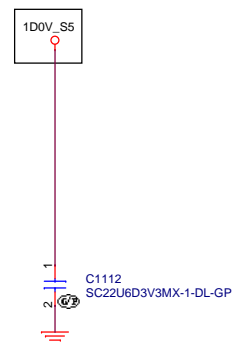
Model: 160 MS SKU1

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Rev	SC
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CPU (Power CAP1)  
Jed15/17" CML

PCH DERIVED RAILS UNSLICED GT VCCIO

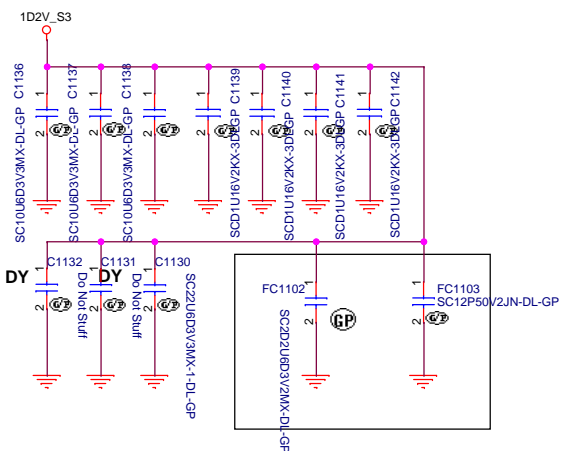


Layout Note:

```

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

```



## <Core Design>



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Title

**CPU (Power CAP2)**Size  
A3

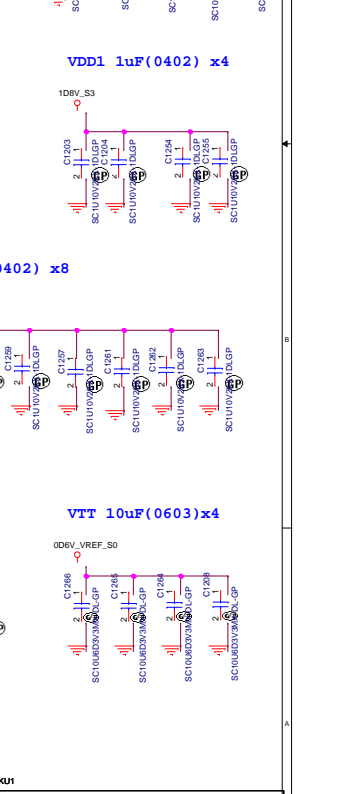
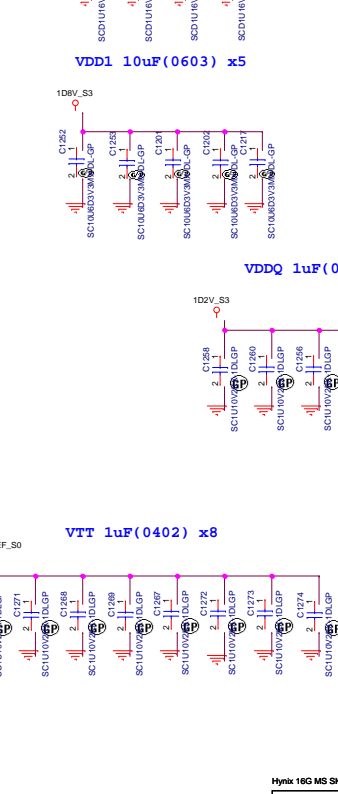
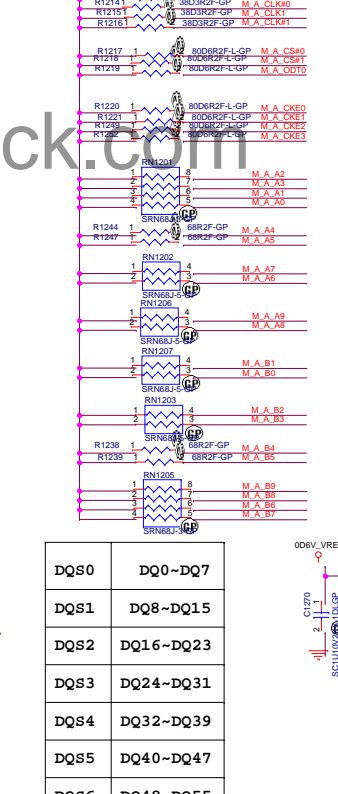
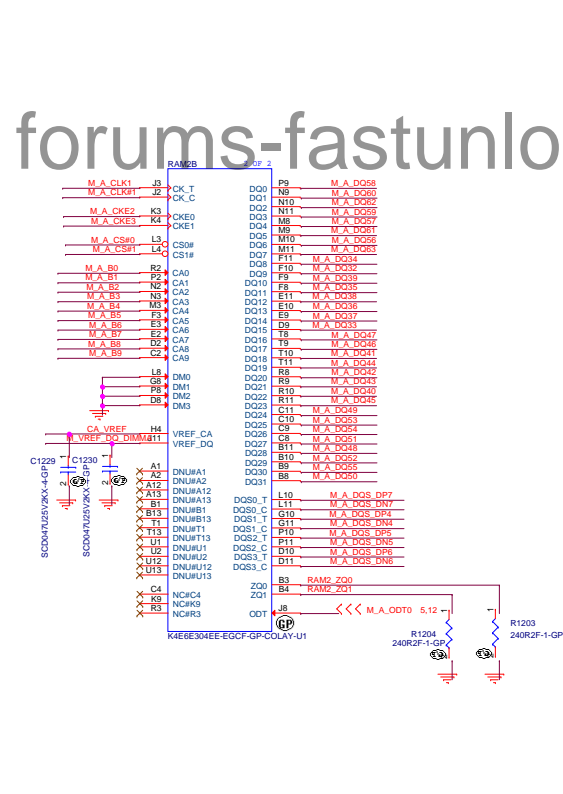
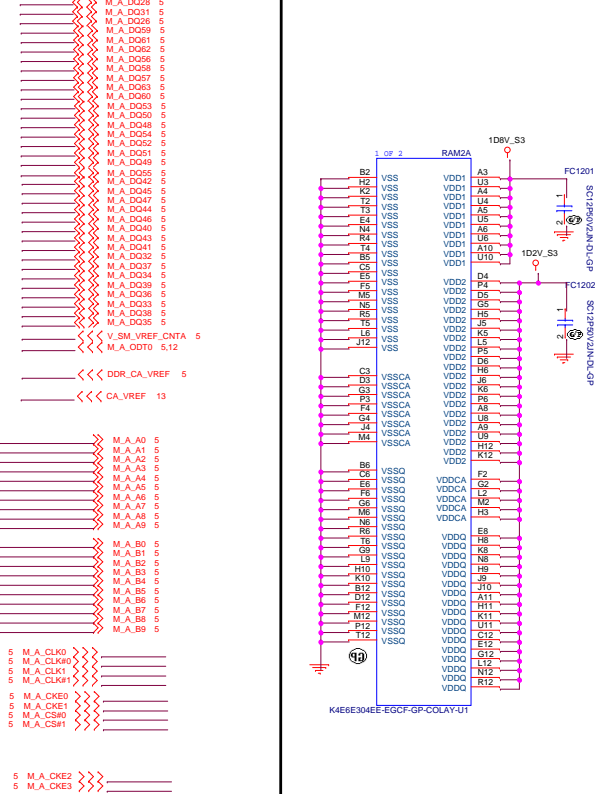
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DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63



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Pin Func = PCH

- 15.77 SPI0\_00 <<<<
- 16 SPI0\_01 <<<<
- 17 CPU\_000\_ALERT# <<<<
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- 100 CPU\_000\_ALERT# <<<<

GPP_B14 / SPKR	No Reboot	Rising edge of PCH_PWROK
----------------	-----------	--------------------------

This signal has a weak internal pull-down.

0 = Disable "No Reboot" mode. (Default)

1 = Enable "No Reboot" mode. (PCH\_PWROK is high)

Notes:

- The internal pull-down is disabled after PCH\_PWROK is high.
- The signal is in the primary well.

GPP_B18 / GSPID_MOSI	No Reboot	Rising edge of PCH_PWROK
----------------------	-----------	--------------------------

This signal has a weak internal pull-down.

0 = Disable "No Reboot" mode. (Default)

1 = Enable "No Reboot" mode. (PCH\_PWROK is high)

Notes:

- The internal pull-down is disabled after PCH\_PWROK is high.
- This signal is in the primary well.

GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#
--------------------	---------------------	------------------------

This signal has a weak internal pull-down.

0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

Notes:

- The internal pull-down is disabled after RSMRST# de-asserts.
- This signal is in the primary well.

GPP_D22 / GSPID_000	Reserved	Rising edge of PCH_PWROK
---------------------	----------	--------------------------

This signal has a weak internal pull-down.

0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

Notes:

- The internal pull-down is disabled after RSMRST# de-asserts.
- This signal is in the primary well.

GPP_CS / SMLALERT#	eSPI or LPC	Rising edge of RSMRST#
--------------------	-------------	------------------------

This signal has a weak internal pull-down.

0 = LPC is selected (for EC). (Default)

1 = eSPI is selected (for EC).

Notes:

- The internal pull-down is disabled after RSMRST# de-asserts.
- This signal is in the primary well.

Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled).

SPIO_MOSI	Reserved	Rising edge of RSMRST#
-----------	----------	------------------------

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_D12 / ISH_SPI_MOSI / GSPID_MOSI	Reserved	Rising edge of RSMRST#
-------------------------------------	----------	------------------------

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_B23 / SMLALERT# / PCHHOT#	Intel® DCI-DOB	Rising edge of RSMRST#
-------------------------------	----------------	------------------------

This signal has a weak internal pull-down.

0 = Disable Intel® DCI-DOB (Default)

1 = Enable Intel® DCI-DOB

Notes:

- The internal pull-down is disabled after RSMRST# de-asserts.
- When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.
- This signal is in the primary well.

SPIO_102	Reserved	Rising edge of RSMRST#
----------	----------	------------------------

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPIO_103	Reserved	Rising edge of RSMRST#
----------	----------	------------------------

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

HDA_SDO / I2SD0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK
---------------------	------------------------------------	--------------------------

This signal has a weak internal pull-down.

0 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

Notes:

- The internal pull-down is disabled after PCH\_PWROK is high.
- This signal is in the primary well.

GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK
--------------------------------------------	-------------------------	--------------------------

This signal has a weak internal pull-down.

0 = Port B is not detected. (Default)

1 = Port B is detected.

Notes:

- The internal pull-down is disabled after PCH\_PWROK is high.
- This signal is in the primary well.

GPP_E21 / DDPB_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK
-------------------------	-------------------------	--------------------------

This signal has a weak internal pull-down.

0 = Port C is not detected. (Default)

1 = Port C is detected.

Notes:

- The internal pull-down is disabled after PCH\_PWROK is high.
- This signal is in the primary well.

GPP_E23 / DDPB_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK
-------------------------	-------------------------	--------------------------

This signal has a weak internal pull-down.

0 = Port D is not detected. (Default)

1 = Port D is detected.

Notes:

- The internal pull-down is disabled after PCH\_PWROK is high.
- This signal is in the primary well.

GPP_H17	Reserved	Rising edge of PCH_PWROK
---------	----------	--------------------------

This signal has a weak internal pull-down.

0 = Port D is not detected. (Default)

1 = Port D is detected.

Notes:

- The internal pull-down is disabled after PCH\_PWROK is high.
- This signal is in the primary well.

GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#
---------	-----------------------	------------------------

This signal has a weak internal pull-down.

0 = 38.4 MHz XTAL frequency selected. (Default)

1 = 24MHz XTAL frequency selected.

Notes:

- The internal pull-down is disabled after RSMRST# de-asserts.
- This signal is in the primary well.

GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#
---------------------	---------------------	------------------------

An external pull-up or pull-down is required.

0 = Integrated CNV enable.

1 = Integrated CNV disable.

INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level
------------	-------------	--------------------------------------------------------

External pull-up or pull-down is required.

0 = 3.3V supply is 3.3V +/- 5%

1 = 3.3V supply is 3.0V +/- 5%

Note: This strap should only be used for specific targeted 1S battery systems.

GPD7	Reserved	Rising edge of DSW_PWROK
------	----------	--------------------------

External pull-up is required. Recommend 100K.

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#
---------	-------------------------	------------------------

This signal has a weak internal pull-down.

0 = Master Attached Flash Sharing (MAFS) enabled. (Default)

1 = Slave Attached Flash Sharing (SAFS) enabled.

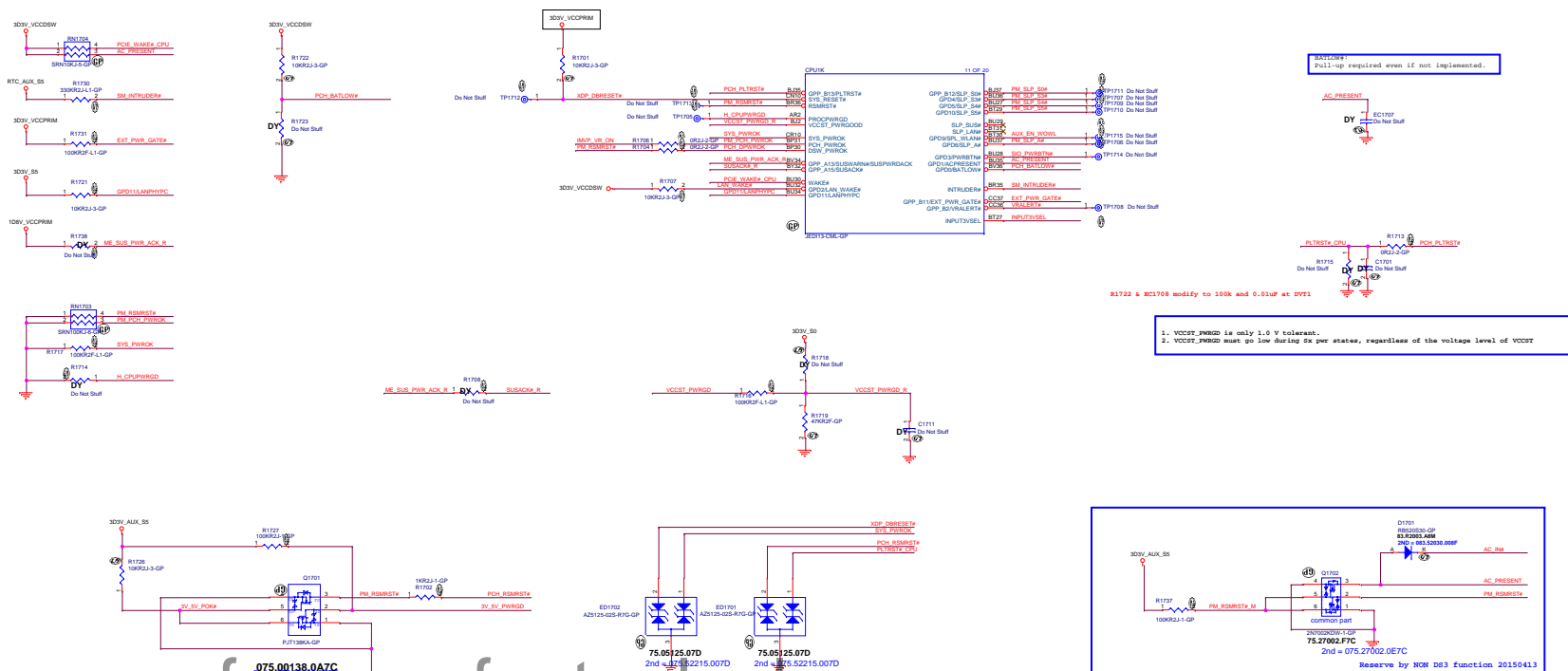
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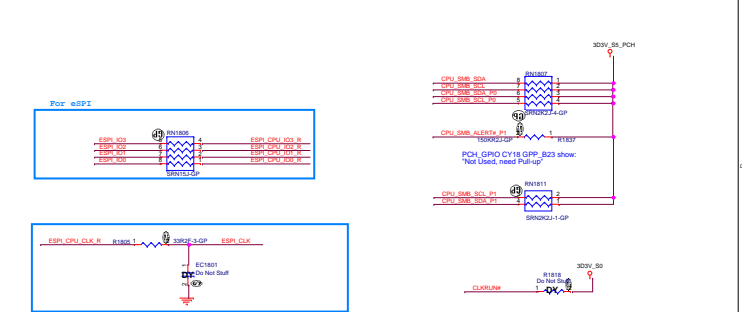
- The internal pull-down is disabled after RSMRST# de-asserts.
- This signal is in the primary well.

Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled).

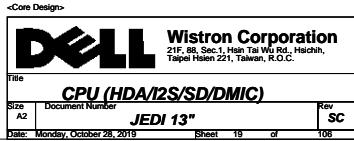


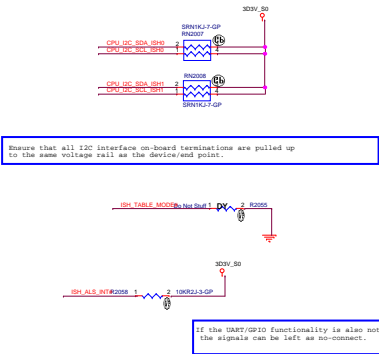
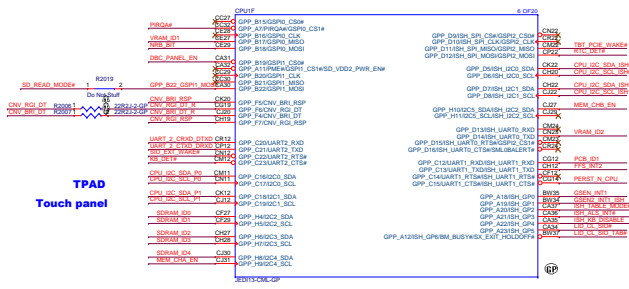
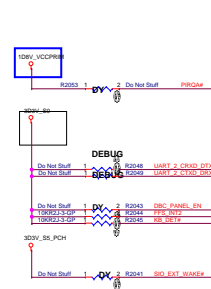






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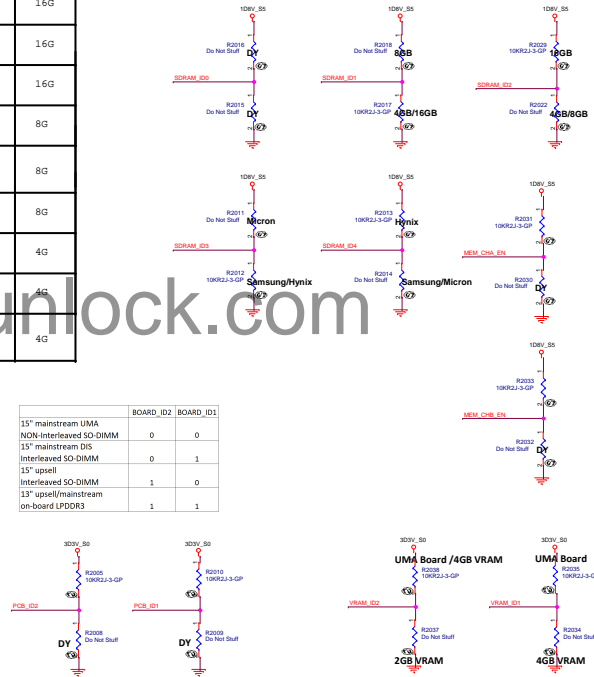




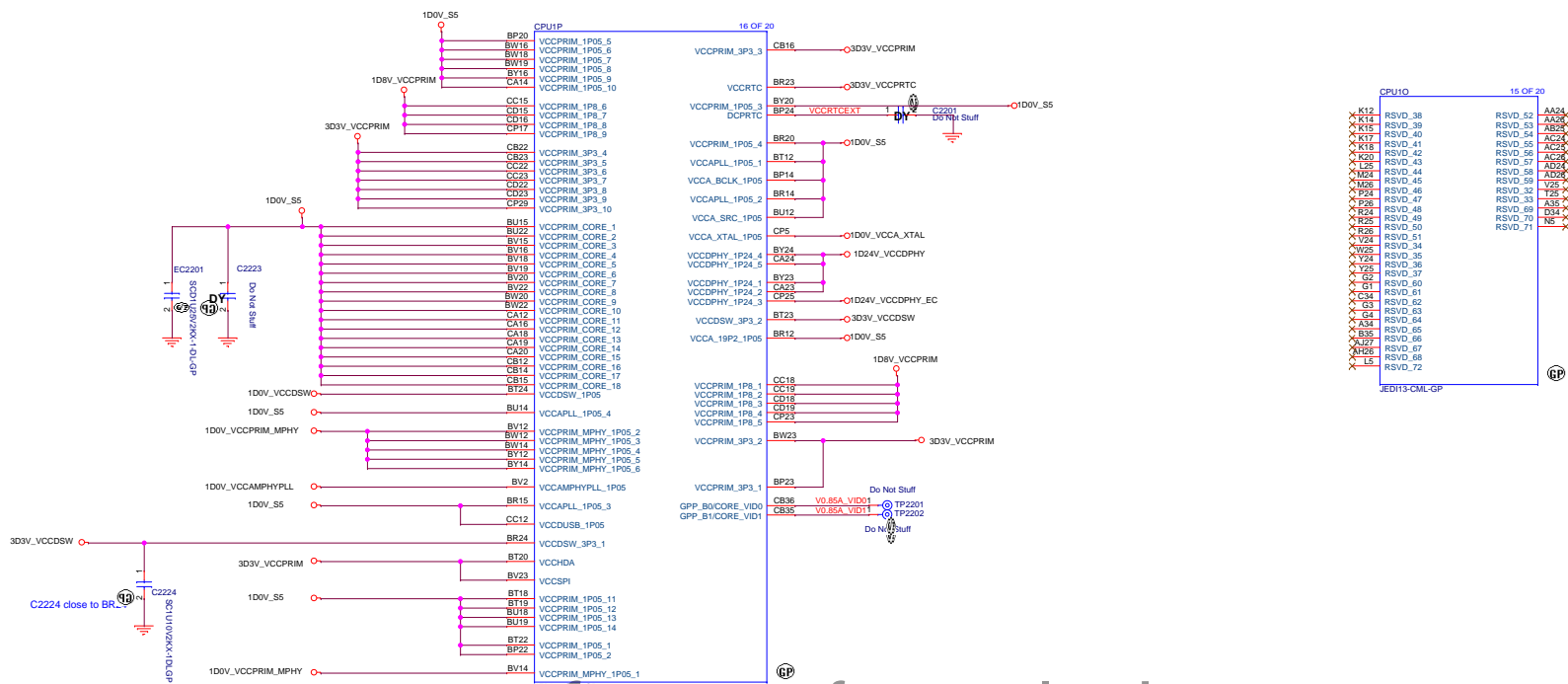
RAM ID						
Vender	MEM_CONFIG [0]	MEM_CONFIG[1:2]	MEM_CONFIG[3:4]	Mér. PN	Wistron. P/N	Capacity
Samsung	NA	01	00	K4AAG165NB-MCRC	TBD	16G
Micron	NA	01	10	MT40A1G16KNR-075E	TBD	16G
Hynix	NA	01	01	H5ANAG6NAMR-UHC	TBD	16G
Samsung	NA	10	00	K4A8G165NB-BCRC	TBD	8G
Micron	NA	10	10	MT40A512M16LY-075R	TBD	8G
Hynix	NA	10	01	H5AN8G6NAFR-UHC	TBD	8G
Samsung	NA	00	00	K4R4G165NE-BCRC	072.44165.0B0U	4G
Micron	NA	00	10	MT40A256M16B2-083R	072.40256.0A0U	4G
Hynix	NA	00	01	H5AN4G6NBJR-UHC	TBD	4G

MEM_CONFIG[4:3]	On-board memory config for chip vendor	11	DIMM Design
		10	Hynix
		01	Micron
		00	Samsung
MEM_CONFIG[2:1]	On-board memory config for total memory size per channel	11	N/A
		10	16GB
		01	8GB
		00	4GB
MEM_CONFIG[0]	Reserved (non-use)		

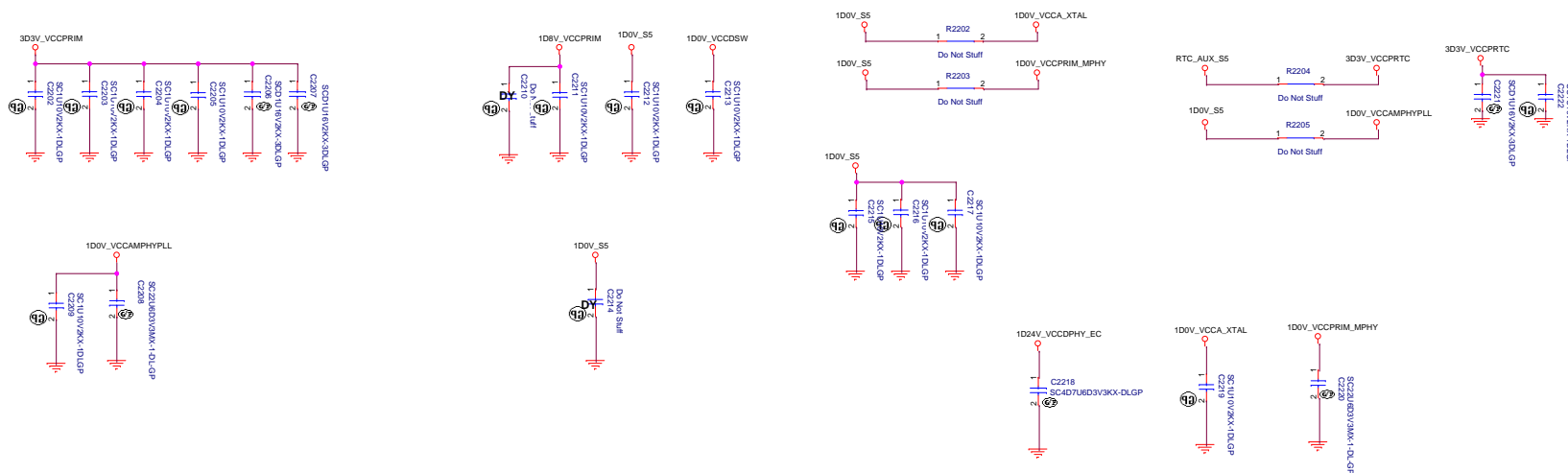
	BOARD_ID2	BOARD_ID1
15" mainstream UMA		
NON-Interleaved SO-DIMM	0	0
15" mainstream DIS		
Interleaved SO-DIMM	0	1
15" upsell		
Interleaved SO-DIMM	1	0
13" upsell/mainstream		
on-board LPDDR3	1	1



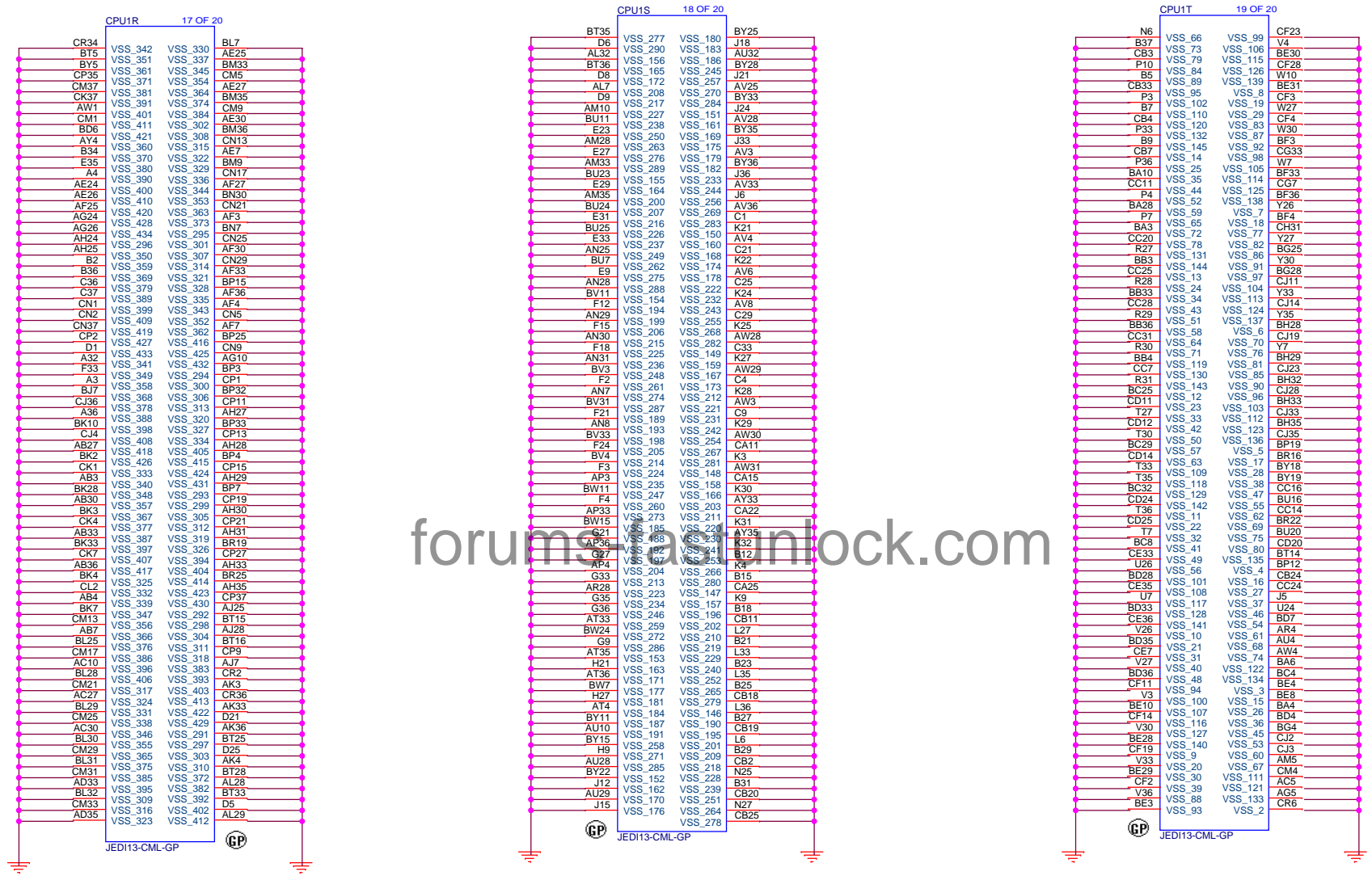




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Main Func = PCH



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Title: **CPU (VSS)**

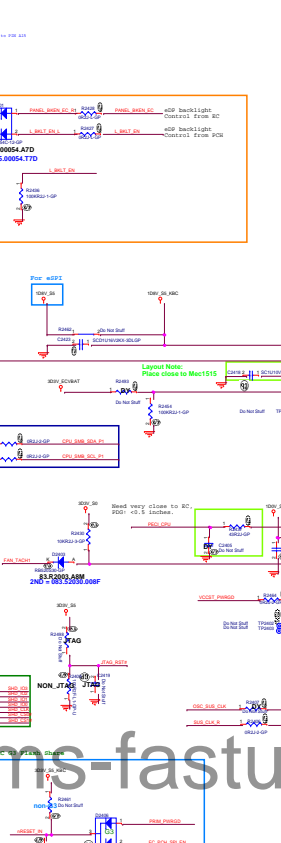
Size: A3 Document Number: **JEDI 13"** Rev: **SC**

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#### 2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD\_C50# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, GPIO055/SHD\_C50# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD\_C50# pin on the board if the Shared SPI flash interface is used on this the SPI\_C50# is selected bios/bootable. [DSMUR020Jc.kicpwr](#)



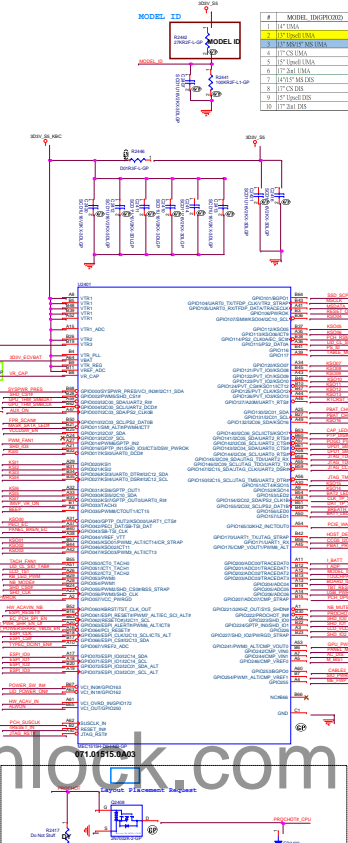
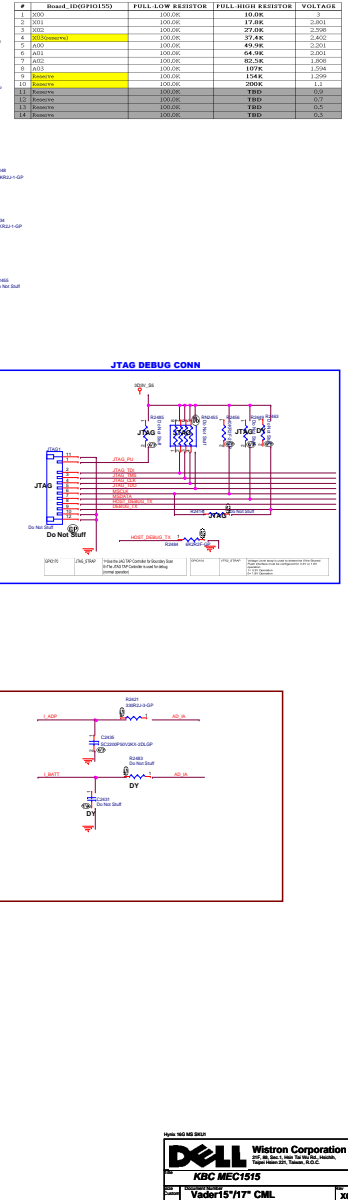
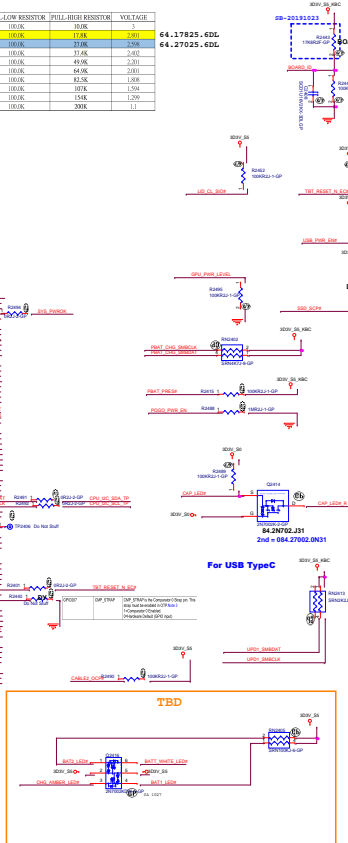
**MODEL: TD**

**MODEL: E2**

**LED POWER RATING**

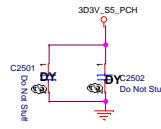
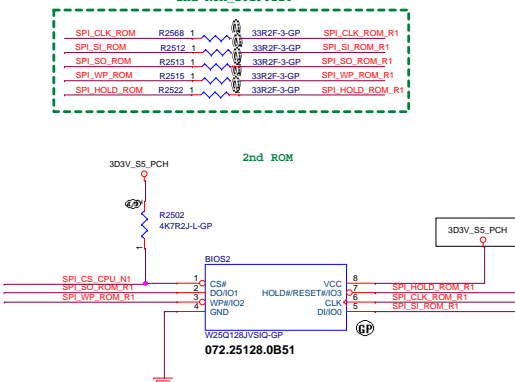
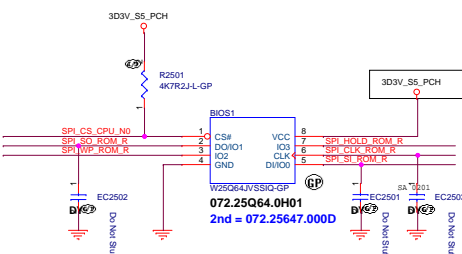
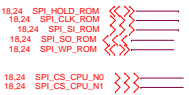
1	2	3	4	5	6	7	8	9	10
1	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
2	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
3	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
4	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
5	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
6	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
7	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
8	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
9	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
10	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

**Power Switch Logic (PSL)**

[illegible]

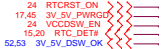


## Main Func = SPI Flash



8M-byte	16M-byte	32M-byte
072.25Q64.0H01	072.25128.0B51	072.25256.0H01
072.25647.000D	072.25127.0B01	072.25256.000D
072.25864.0C01	072.25128.0D61	072.25673.0A01

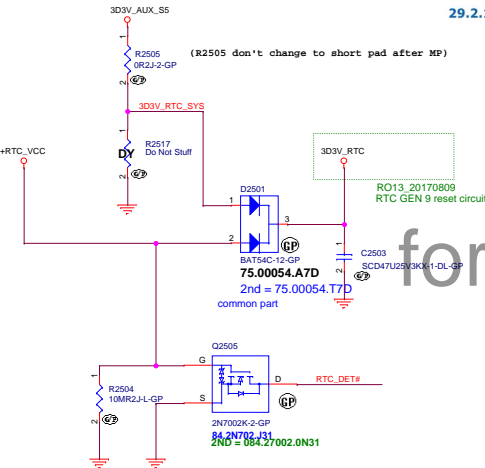
Main Func = RTC



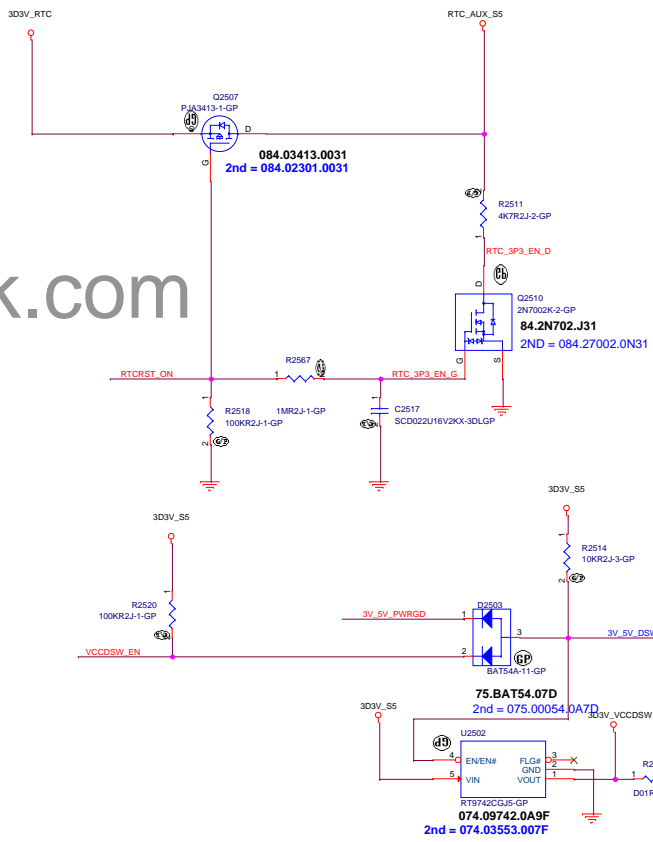
Delivery Voltage 3.19V

### 29.2.1 VCCRTC External Circuit

On RBL, the VCCRTC bias voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW\_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



## RTC



Add RTC GEN 9 reset circuit\_20170809

Hynix 16G MS SKU1



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1

### Flash/RTC

15

L

**JEDI 13'**

1

10

## Slugs

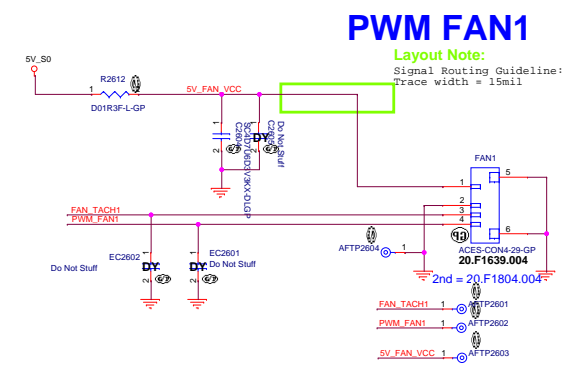
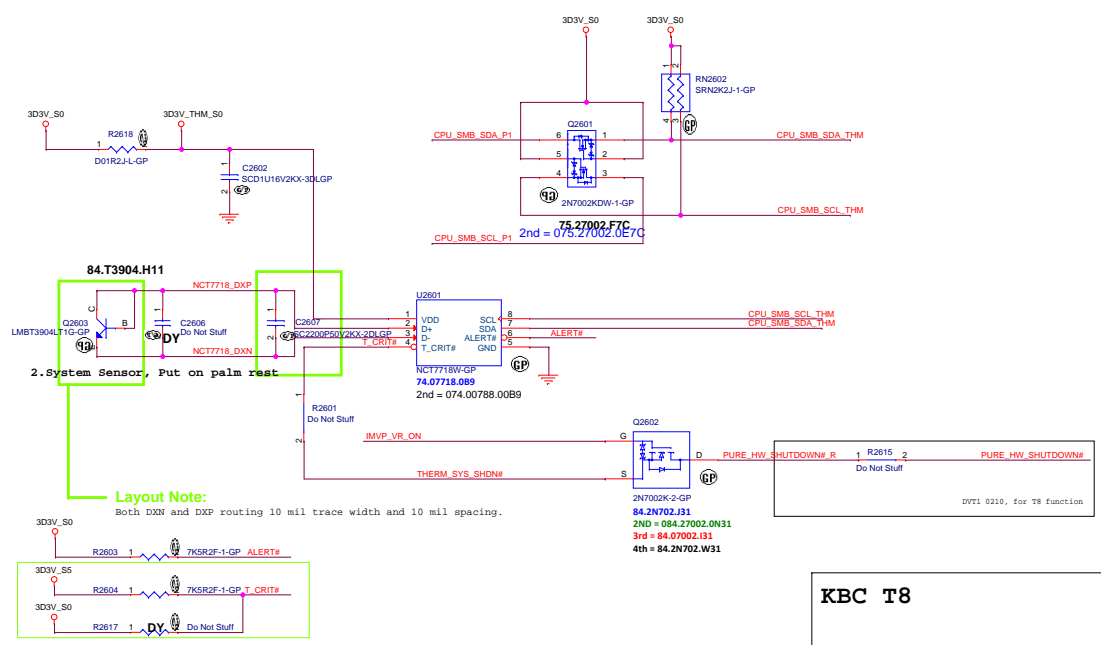
Rev

55

100

Main Func = Thermal Sensor

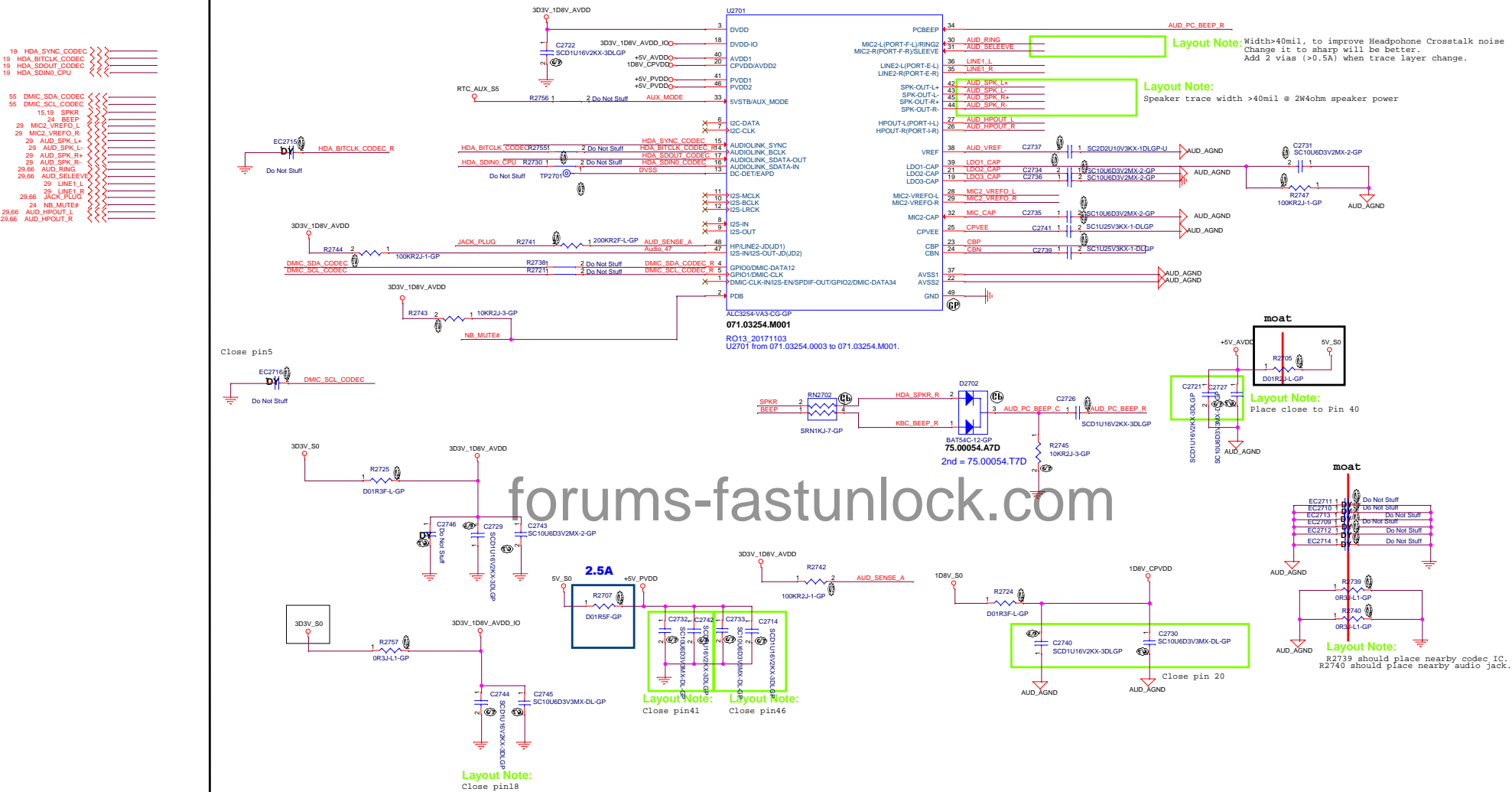
- 18.24.92 CPU\_SMB\_SDA\_P1
- 18.24.92 CPU\_SMB\_SCL\_P1
- 17.40.61.63.71 PLTSTSTV\_CPU
- 17.24 IMVP\_VR\_ON
- 40 PURE\_HW\_SHUTDOWN#
- 24 PWM\_FAN1



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

KBC T8


Close to KBC



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# Main Func = Audio

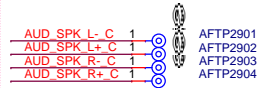
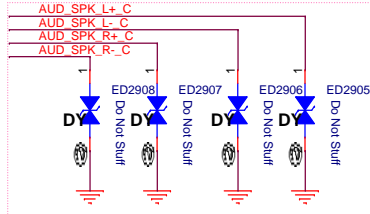
27 AUD\_SPK\_L+ >>>  
27 AUD\_SPK\_L- >>>  
27 AUD\_SPK\_R+ >>>  
27 AUD\_SPK\_R- >>>

21 SPK\_ID <<<  
27 MIC2\_VREFO\_R <<<  
27 MIC2\_VREFO\_L <<<  
27.66 AUD\_RING <<<  
27.66 AUD\_HPOUT\_L <<<  
27 LINE1\_L <<<  
27.66 AUD\_HPOUT\_R <<<  
27 LINE1\_R <<<  
27.66 AUD\_SELEEVE <<<

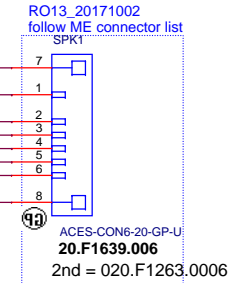
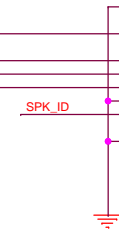
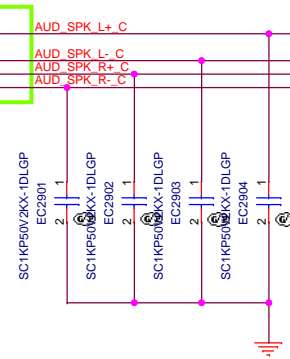
27.66 JACK\_PLUG >>>

## Layout Note:

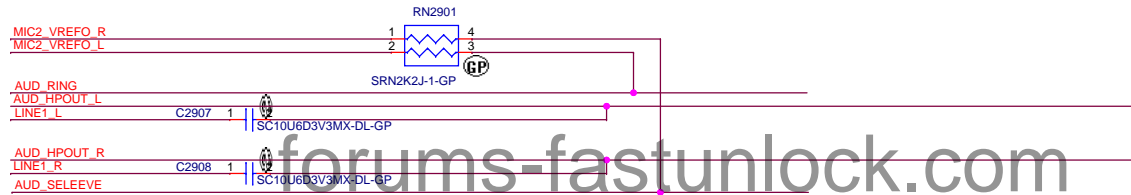
Speaker trace width >40mil @ 2W4ohm speaker power



## Speaker

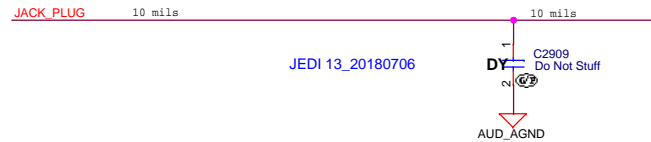


CONN Pin	Net name
Pin1	SPK_L+_C
Pin2	SPK_L-_C
Pin3	SPK_R+_C
Pin4	SPK_R-_C
Pin5	GND
Pin6	SPK_DET#_CON



## Delay circuit

(JACK\_PLUG\_DET: on IO Board)



JEDI 13\_20180706

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A4

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# Main Func = Power Plane & Sequence

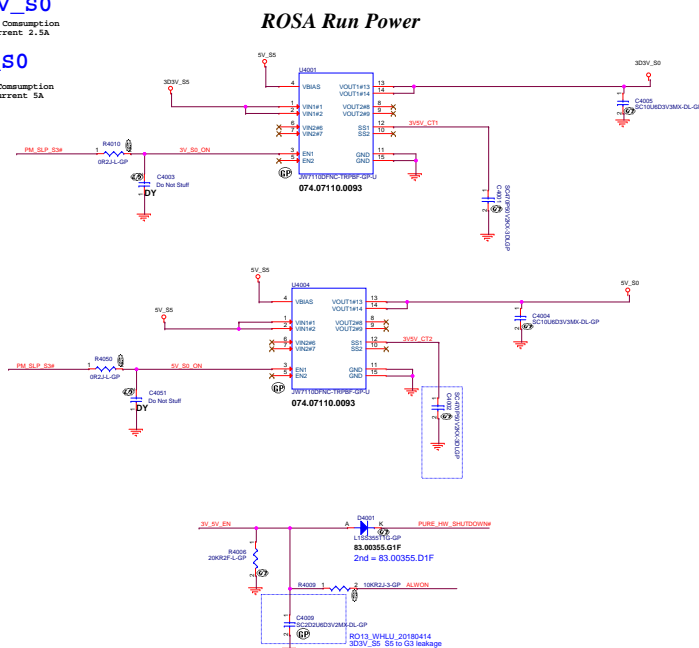
17.51.50.71 PM\_SLP\_S3W >>>  
45 3V\_SV\_5V >>>  
26 PURE\_PWM\_SHUTDOWN >>>  
17.51 PM\_SLP\_S3W >>>  
45 ALDO1 >>>  
17.24.44.48 VCCST\_PWRGD >>>  
24.53 PM\_SLP\_S3W >>>  
52 100V\_S5\_PWRGD >>>  
17.51.50.71 PM\_SLP\_S3W >>>  
21 GPPC\_H18\_VCCIO\_LPM >>>  
17.51.50.71 PM\_SLP\_S3W >>>

## 3D3V\_S0

3D3V\_S0 Consumption  
Peak current 2.5A

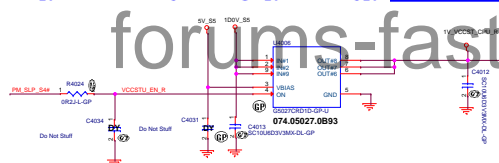
## 5V\_S0

5V\_S0 Consumption  
Peak current 5A



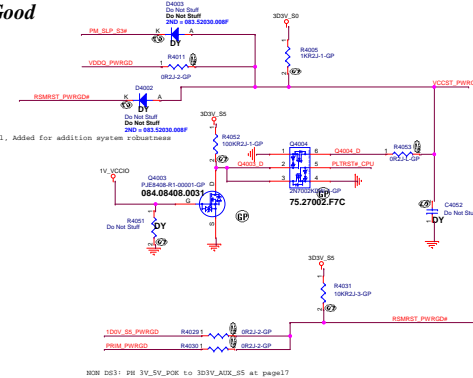
## MANAGEMENT RAIL POWER GENERATION

VCCST\*, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

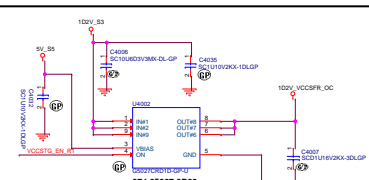


## +V1.8V\_VDD1 LPDDR3

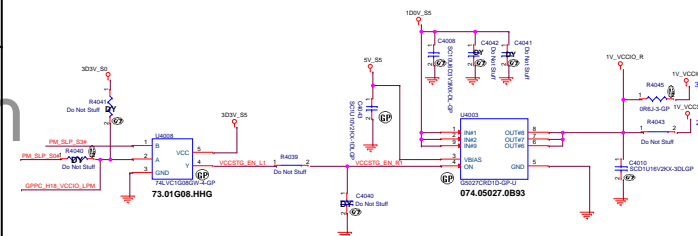
## Power Good



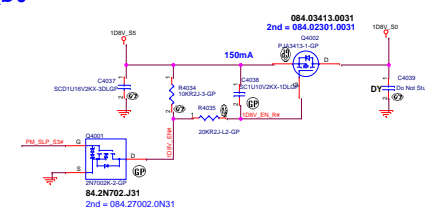
## VCCSFR\_OC



## VCCIO and VCCSTG




## +V1.8V\_S0





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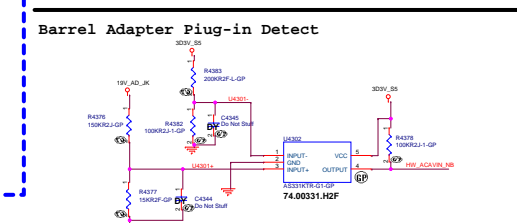
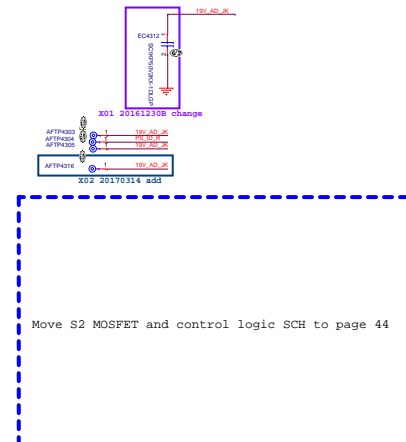
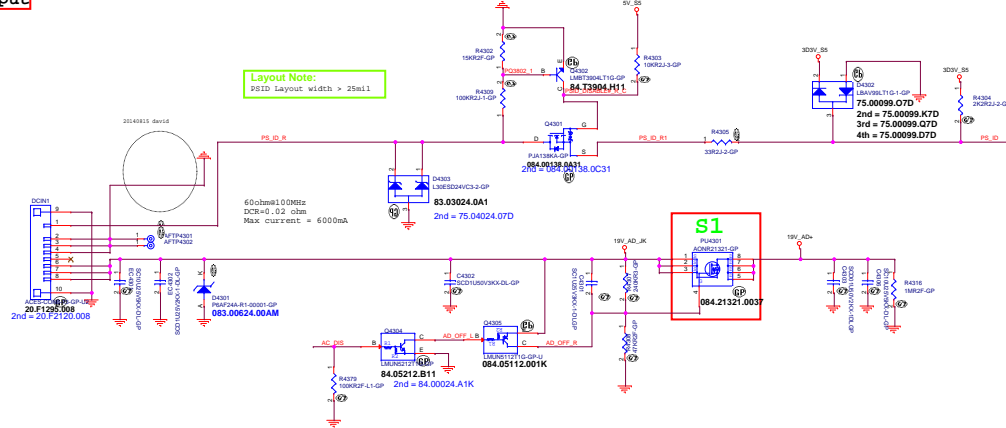
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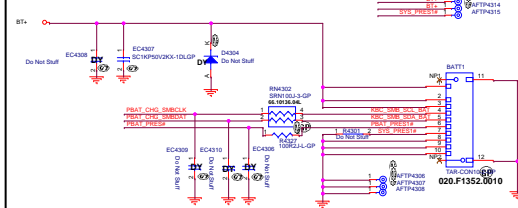
# Main Func = ADT Input

24.44 HW\_ACAVIN\_NB <<<<  
24 PE\_ID <<<<  
17.44 AC\_IN >>>>  
24.44 PRAT\_CHG\_SMBCLK <<<<  
24.44 PRAT\_CHG\_SMBCLK <<<<  
24.44 PRAT\_CHG\_SMBCLK <<<<  
24.44 PRAT\_CHG\_SMBCLK <<<<  
24.44 AC\_IN >>>>



## Main Func = M-BAT Input

Batt Connector



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## ISL9538H For Charger

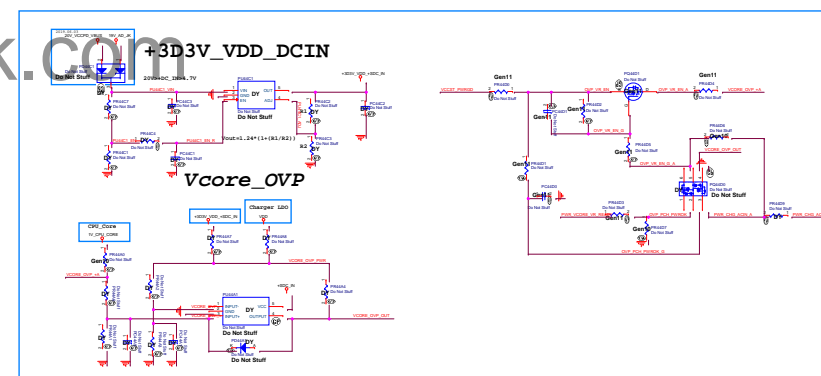
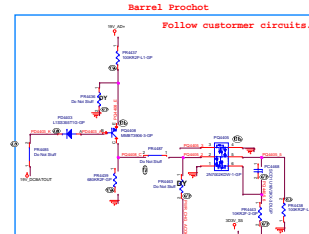
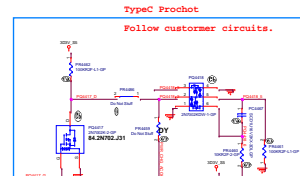
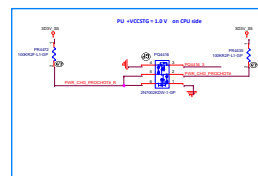
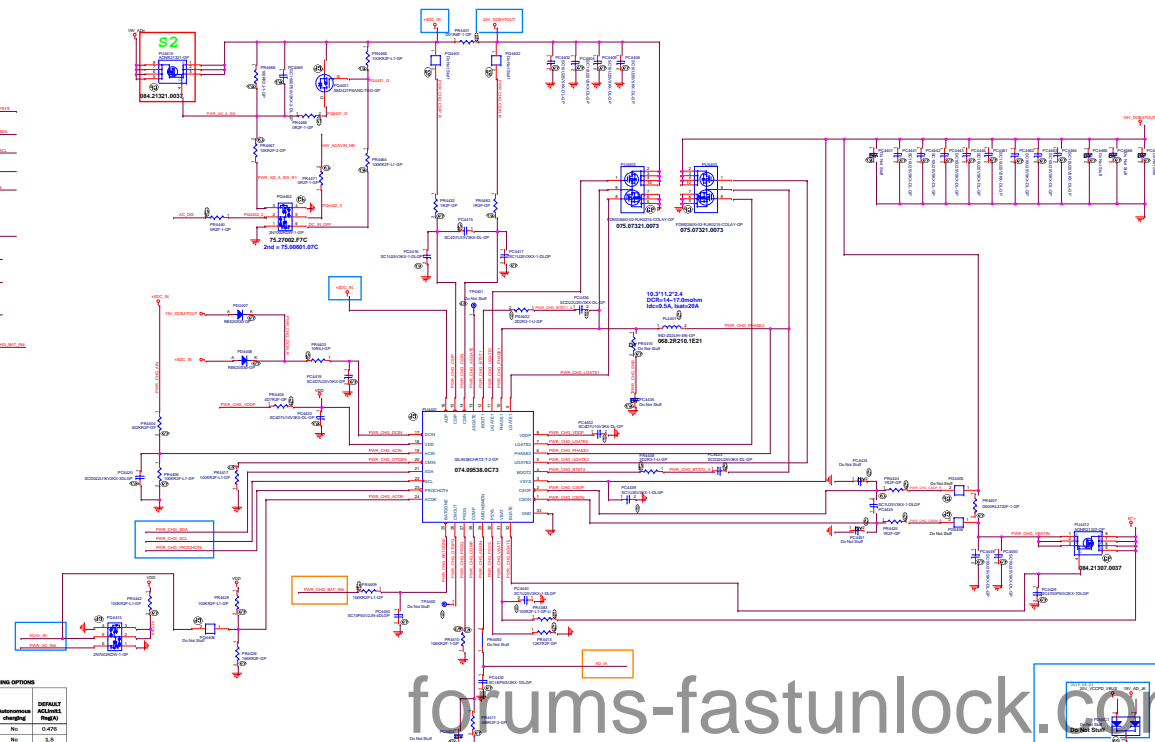
OFFPAGE

ISL9538H (1/1)



TABLE 32. PROG PIN PROGRAMMING OPTIONS

PROG PIN	RESISTANCE (Ω)	MIN	TYP	MAX	CELL #	DEFAULT	OPTIONAL	MINIMUM	MAXIMUM	DEFAULT	ALLOWED
0	0	0	0	0	1	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
8,49	8,49	8,49	8,49	8,49	1	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
14,7	14,7	14,7	14,7	14,7	1	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
25,0	25,0	25,0	25,0	25,0	1	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
26,7	26,7	26,7	26,7	26,7	1	7330Ω	Yes	0.47Ω	0.47Ω	Yes	0.47Ω
35,7	35,7	35,7	35,7	35,7	1	7330Ω	Yes	0.47Ω	0.47Ω	Yes	0.47Ω
43,2	43,2	43,2	43,2	43,2	2	7330Ω	Yes	0.47Ω	0.47Ω	Yes	0.47Ω
62,3	62,3	62,3	62,3	62,3	2	7330Ω	Yes	0.47Ω	0.47Ω	Yes	0.47Ω
63,9	63,9	63,9	63,9	63,9	2	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
75,5	75,5	75,5	75,5	75,5	2	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
82,8	82,8	82,8	82,8	82,8	2	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
83,1	83,1	83,1	83,1	83,1	2	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
105	105	105	105	105	3	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
118	118	118	118	118	3	7330Ω	Yes	0.47Ω	0.47Ω	Yes	0.47Ω
133	133	133	133	133	3	7330Ω	Yes	0.47Ω	0.47Ω	Yes	0.47Ω
147	147	147	147	147	3	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
162	162	162	162	162	3	7330Ω	Yes	0.47Ω	0.47Ω	Yes	0.47Ω
178	178	178	178	178	3	7330Ω	Yes	0.47Ω	0.47Ω	Yes	0.47Ω
196	196	196	196	196	4	7330Ω	Yes	0.47Ω	0.47Ω	Yes	0.47Ω
215	215	215	215	215	4	7330Ω	Yes	0.47Ω	0.47Ω	Yes	0.47Ω
237	237	237	237	237	4	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
261	261	261	261	261	4	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
287	287	287	287	287	4	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
316	316	316	316	316	4	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω
348	348	348	348	348	5	7330Ω	No	0.47Ω	0.47Ω	No	0.47Ω



Rev	<b>A00</b>
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## OFFPAGE



44.46.44 VCCST\_PWRSD <<< VCCST\_PWRSD

## For VCCGT Sense



## For Vcore Sense

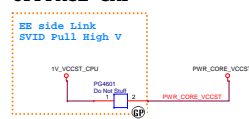


## For VCCSA Sense



44 PWR\_VCORE\_VR\_READY <<< PWR\_VCORE\_VR\_READY

## OFFPAGE-GAP



47 PWR\_VCORE\_PWMA <<<

47 PWR\_VCORE\_IBUM <<<

47 PWR\_VCORE\_IBUM <<<

47 PWR\_VCORE\_FCCM <<<

47 PWR\_VCORE\_PWMA <<<

47 PWR\_VCORE\_FCCM <<<

47 PWR\_VCORE\_IBUM <<<

47 PWR\_VCORE\_IBUM <<<

50 PWR\_VCCSA\_IBUM <<<

50 PWR\_VCCSA\_PWMA <<<

50 PWR\_VCCSA\_FCCM <<<

47 PWR\_VCORE\_IBUM <<<

47 PWR\_VCORE\_IBUM <<<

47 PWR\_VCORE\_IBUM <<<

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47 PWR\_VCORE\_IBUM <<<

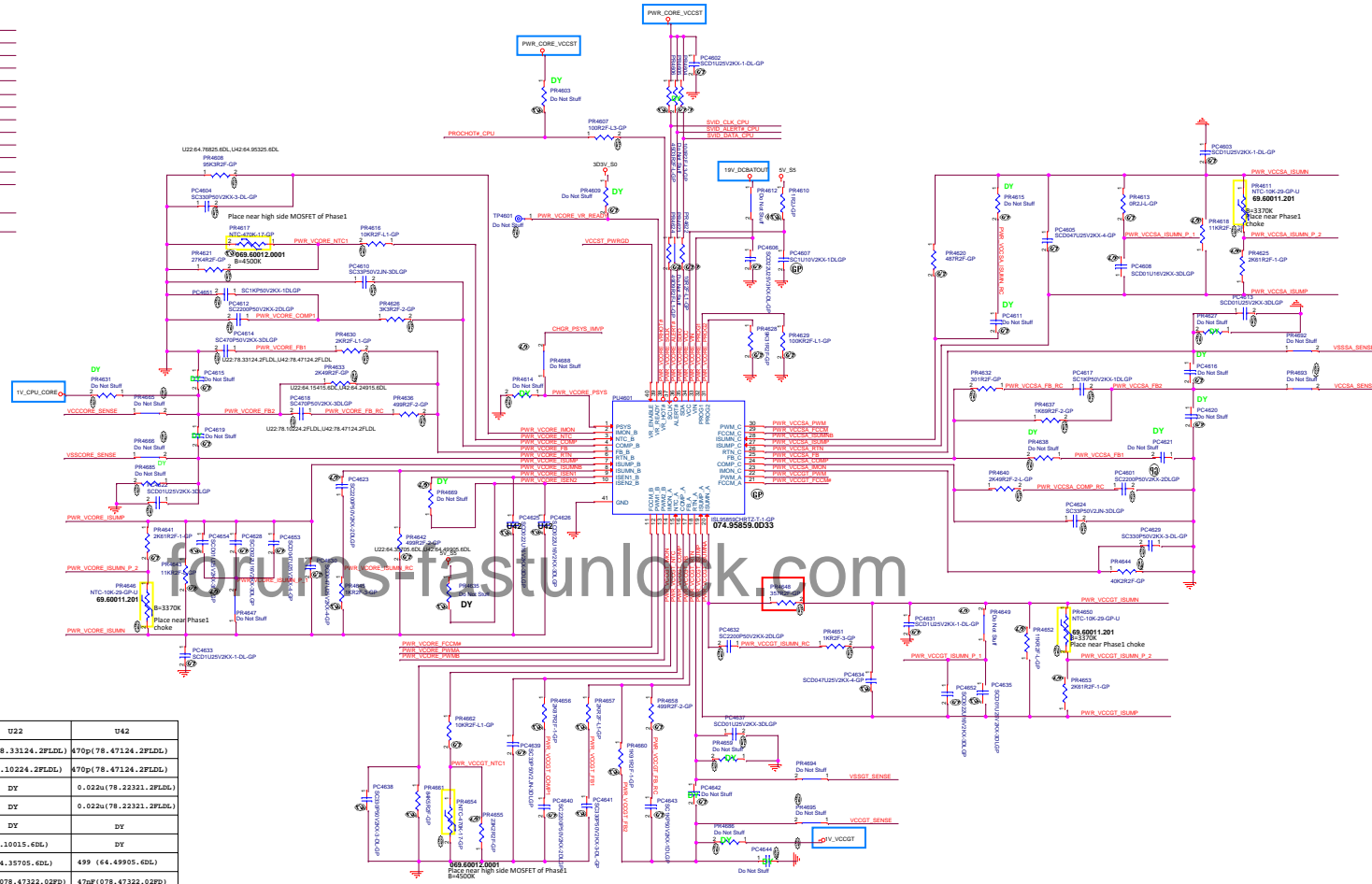
47 PWR\_VCORE\_IBUM <<<

47 PWR\_VCORE\_IBUM <<<

47 PWR\_VCORE\_IBUM <<<

	U22	U42
PC4614	330p(78.33124.2PLDL)	470p(78.47124.2PLDL)
PC4618	1Kp(78.10224.2PLDL)	470p(78.47124.2PLDL)
PC4625	DY	0.022u(78.23321.2PLDL)
PC4626	DY	0.022u(78.23321.2PLDL)
PC4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4642	357(64.35705.6DL)	499(64.49905.6DL)
PC4630	470p(78.47322.02PD)	470p(78.47322.02PD)
PC4628	230p(78.23321.2PLDL)	230p(78.23321.2PLDL)
PC4654	100p(78.10332.2PLDL)	100p(78.10332.2PLDL)
PC4653	DY	470p(78.47322.02PD)
PR4633	1.58K(64.15415.6DL)	2.49K(64.24915.6DL)
PR4608	76.8K(64.76825.6DL)	95.3K(64.95325.6DL)


## ISL95859C For CPUCORE

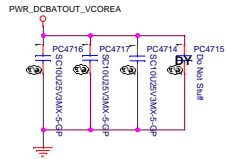
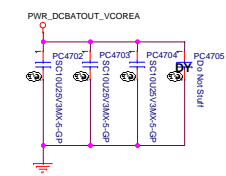
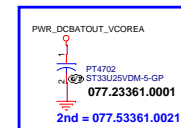
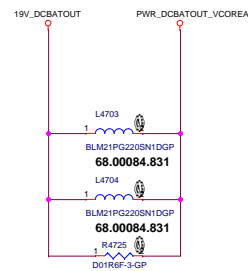


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# AOZ5038QI For VCORE

For acoustic noise

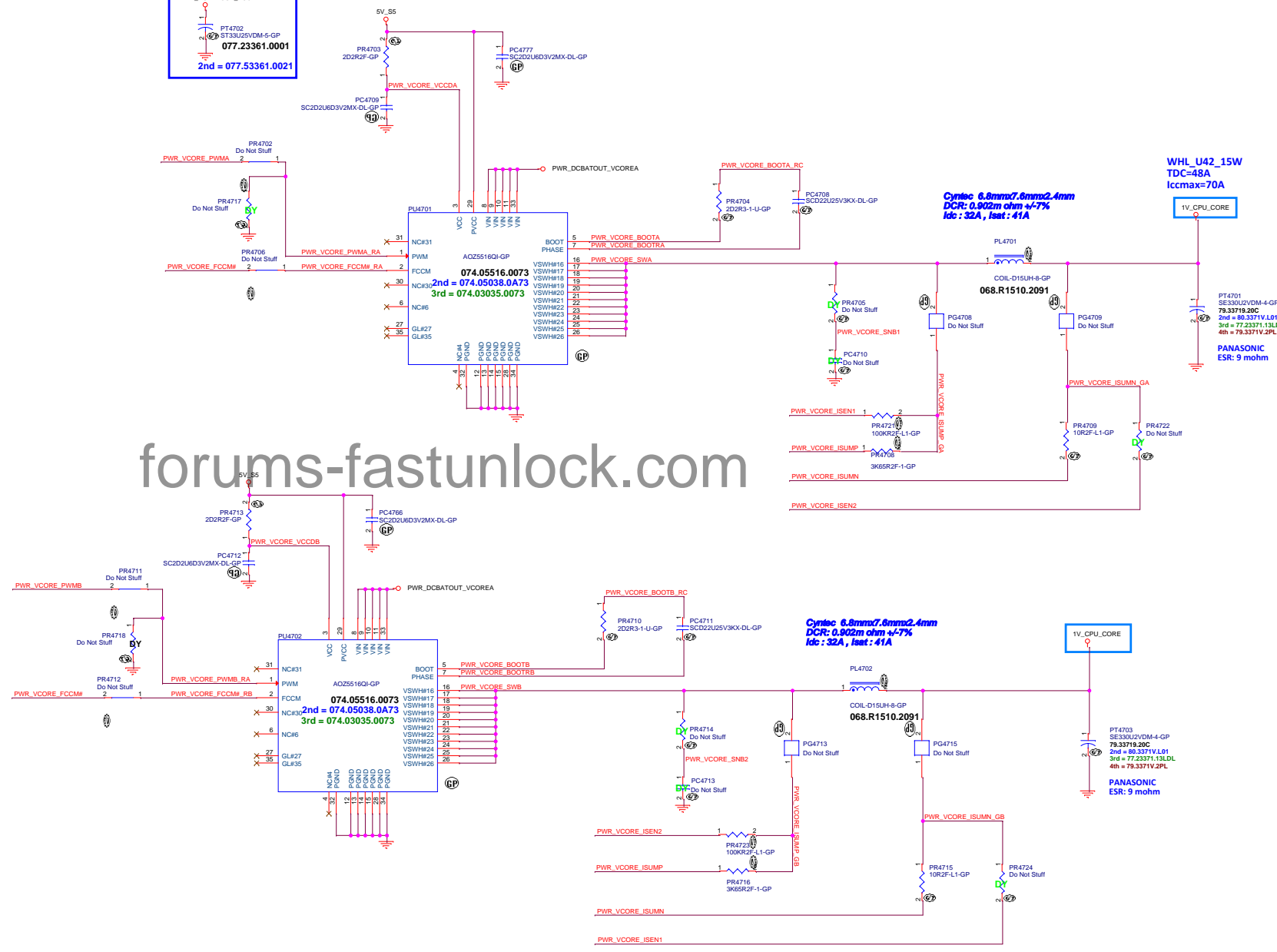
46	PWR_VCORE_PWMA	
46,47	PWR_VCORE_FCCM#	
46,47	PWR_VCORE_ISEN1	
46,47	PWR_VCORE_ISUMP	
46,47	PWR_VCORE_ISUMN	
46,47	PWR_VCORE_ISEN2	



```

46      PWR_VCORE_PWMB
46,47    PWR_VCORE_FCCM#
46,47    PWR_VCORE_ISEN2
46,47    PWR_VCORE_ISUMP
46,47    PWR_VCORE_ISUMN
46,47    PWR_VCORE_ISEN1

```

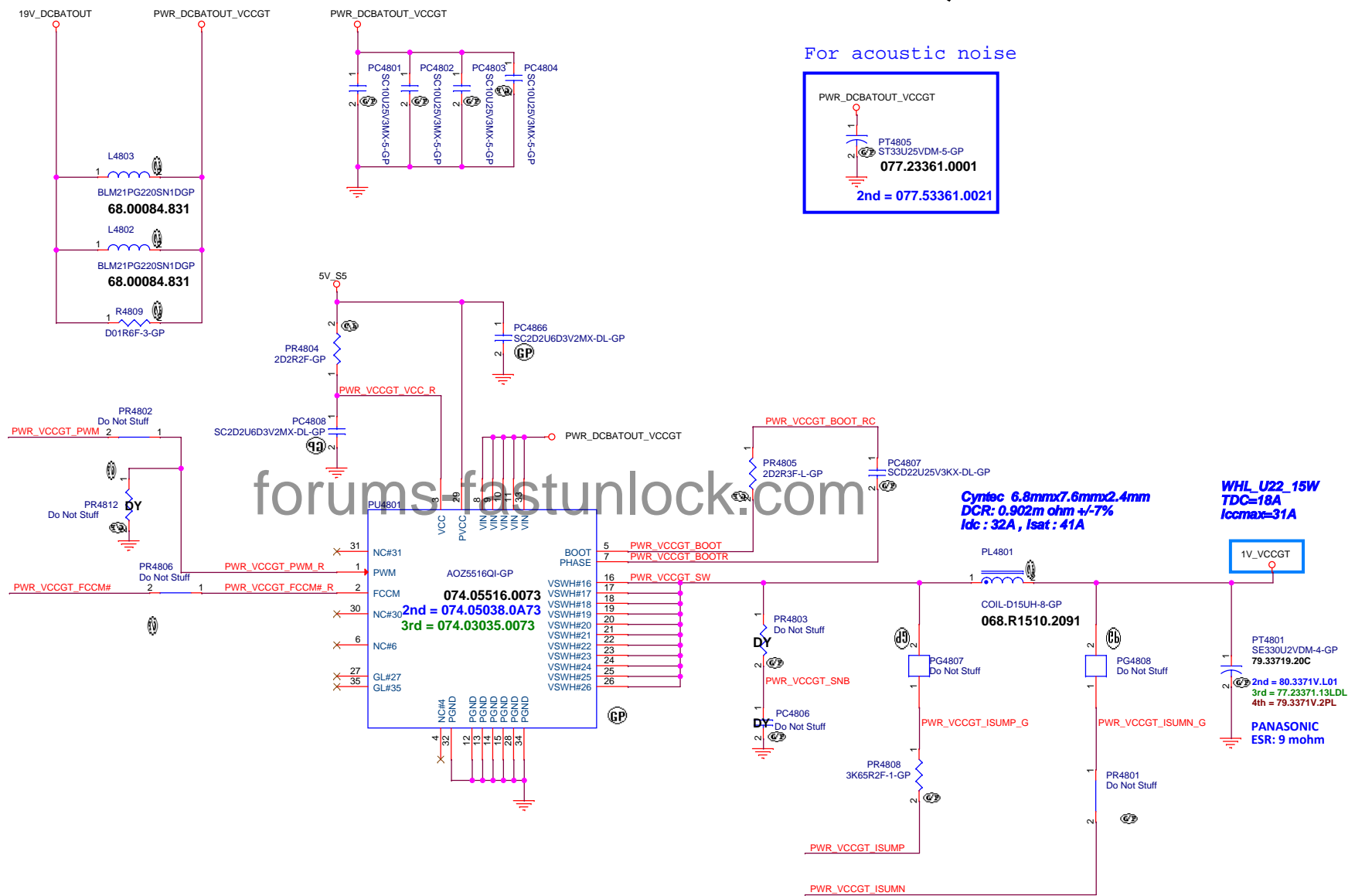
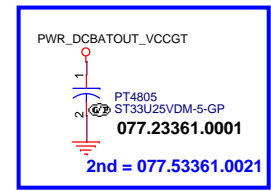


Offpage-Signal

- 46 PWR\_VCCGT\_PWM
- 46 PWR\_VCCGT\_FCCM#
- 46 PWR\_VCCGT\_ISUMP
- 46 PWR\_VCCGT\_ISUMN

# AOZ5038QI For VCCGT


For acoustic noise





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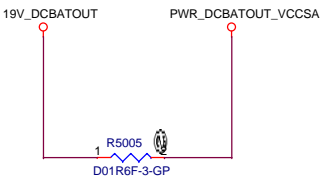
Hynix 16G MS SKU1

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>CPU_VCCGTUS</b>		
Size A4	Document Number <b>Unicorn_LV530_KBL_MB14</b>	Rev <b>SC</b>
Date: Monday, October 28, 2019		Sheet 49 of 106

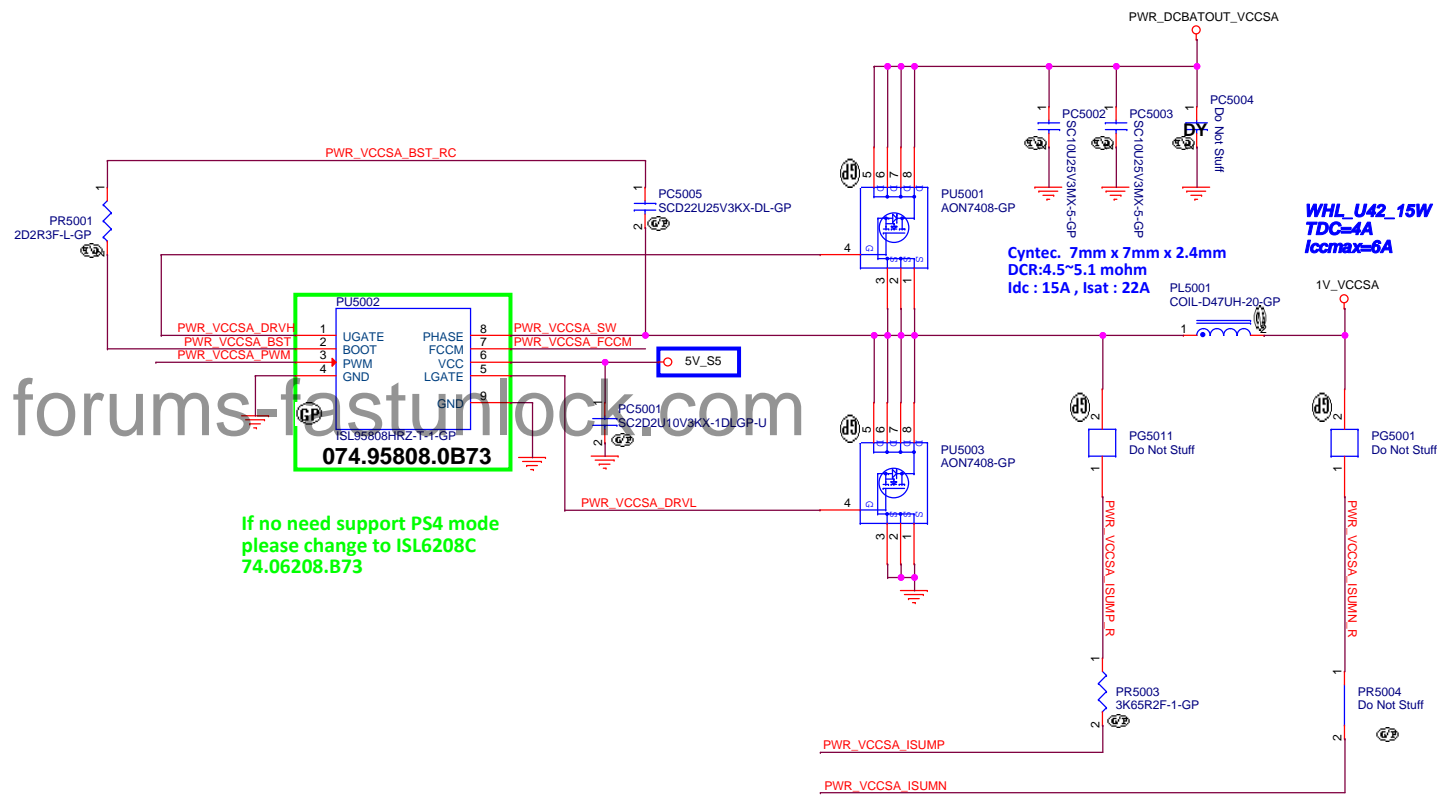
OFFPAGE-Signal

46 PWR\_VCCSA\_PWM >>>—  
46 PWR\_VCCSA\_FCCM >>>—  
46 PWR\_VCCSA\_ISUMP <<<—  
46 PWR\_VCCSA\_ISUMN <<<—

OFFPAGE-GAP

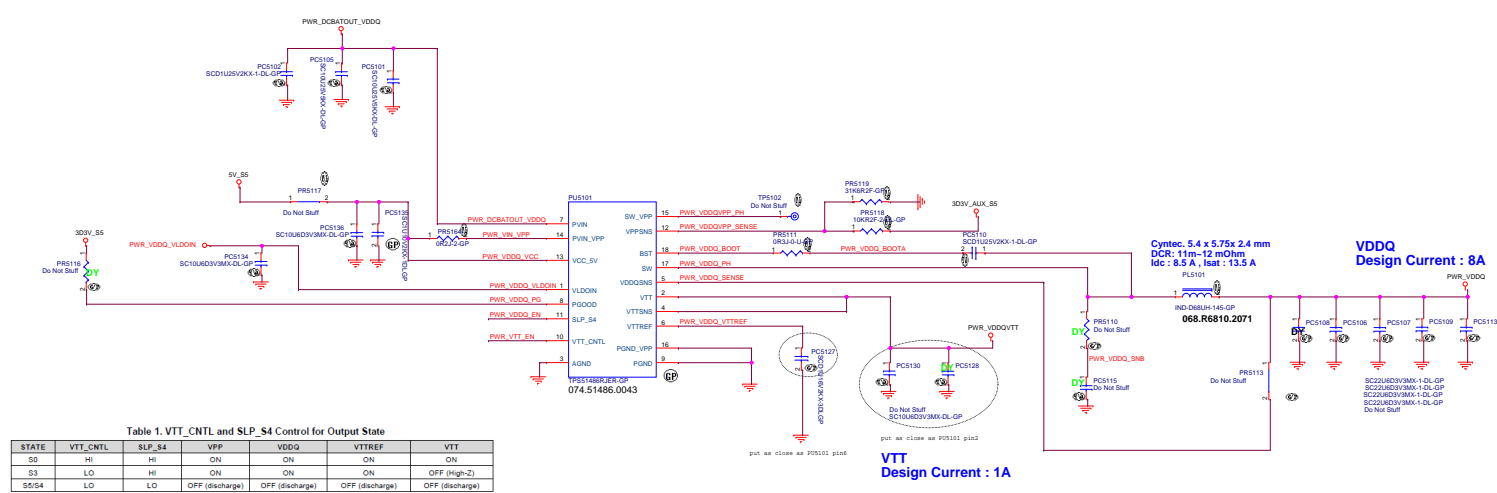
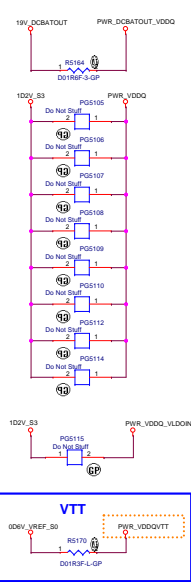
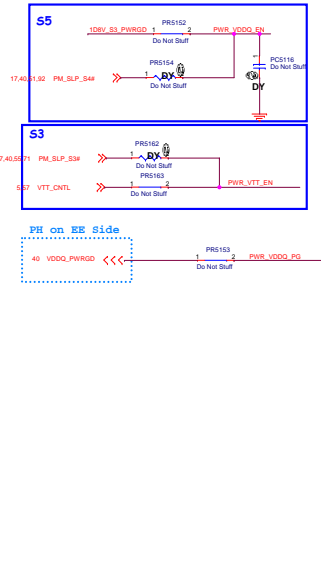


# ISL95808 For VCCSA



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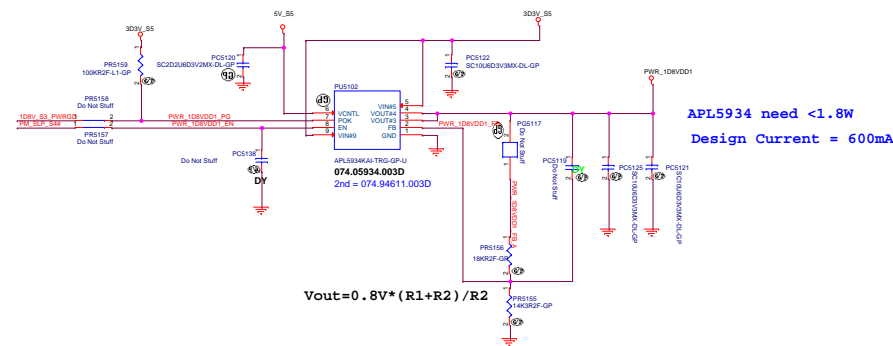
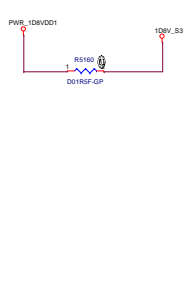
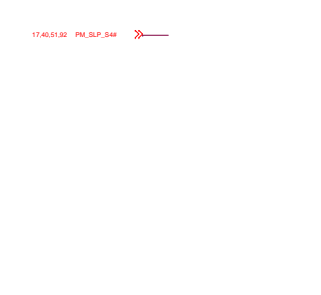
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## OFFPAGE-Signal

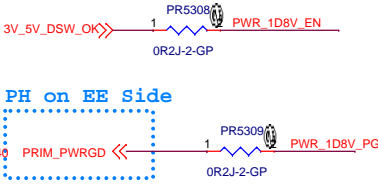
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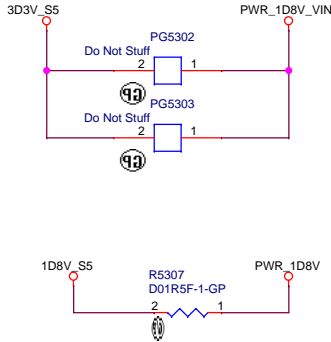


Main Func = 1D8V

OFFPAGE

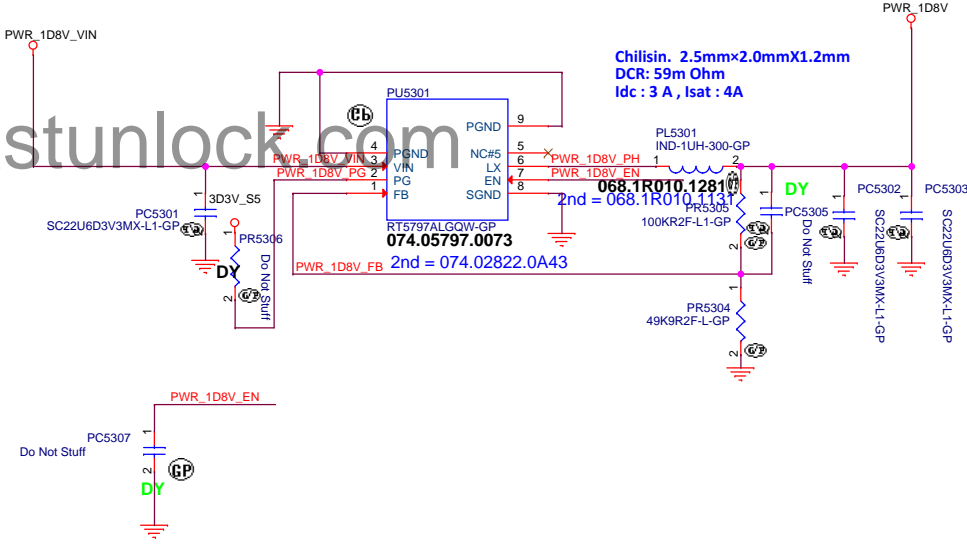


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RT5797AL for 1D8V


Design Current=1.965A  
Icc(max)=2.165A  
OCP>3A



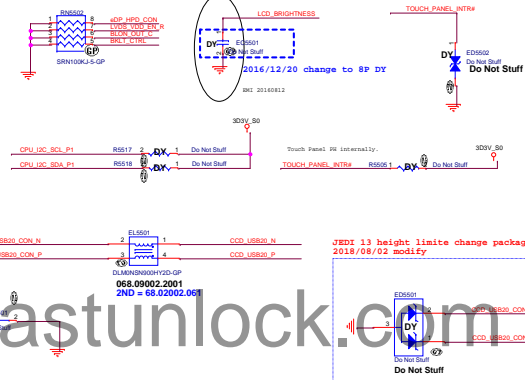
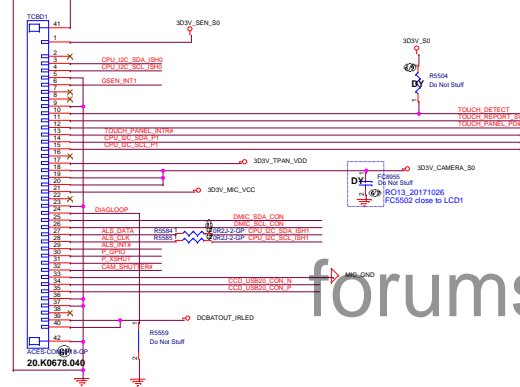
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Title <b>(Reserved)</b>			
Size A4	Document Number <b>JEDI 13"</b>		Rev <b>SC</b>
Date: Monday, October 28, 2019		Sheet 54 of	106

## Sensor/TOUCH PANEL/IR Camera

[illegible]

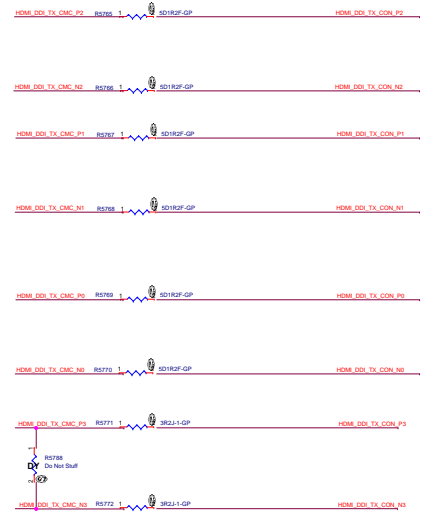
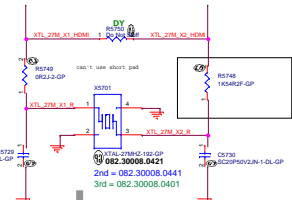
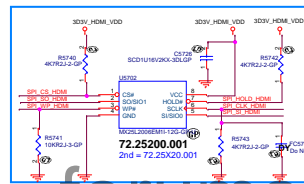
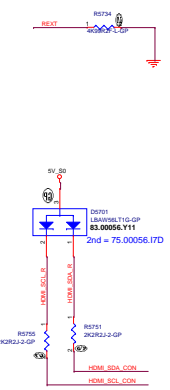
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<Core Design>

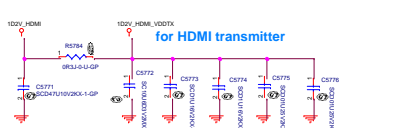
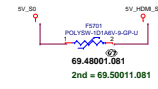
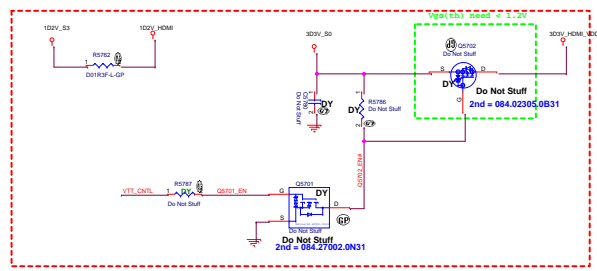
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Title <b>(Reserved)</b>			
Size A4	Document Number <b>JEDI 13"</b>		Rev <b>SC</b>
Date: Monday, October 28, 2019		Sheet 56 of	106



5,51 VTT\_CNTL >>>



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[illegible]

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<Core Design>

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Size A4	Document Number <b>JEDI 13"</b>	Rev
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-Core Design-			
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size	Document Number		Rev
A2	JEDI 13"		SC
Date:	Monday, October 26, 2019		Sheet 60 of 106

Main Func = WLAN

3 BLUETOOTH\_EN >>>  
21 WIFI\_RF\_EN >>>  
17,40,63,71 PLTRST#\_CPU >>>

18,24 SUS\_CLK\_R >>>

20 CNV\_BRI\_DT >>>  
20 CNV\_RGI\_RSP >>>  
15,20 CNV\_RGI\_DT >>>

20 CNV\_BRI\_RSP >>>  
21 CNV\_WT\_CLK\_DP >>>  
21 CNV\_WT\_CLK\_DN >>>

21 CNV\_WT\_DP0 >>>  
21 CNV\_WT\_DN0 >>>  
21 CNV\_WT\_DP1 >>>  
21 CNV\_WT\_DN1 >>>

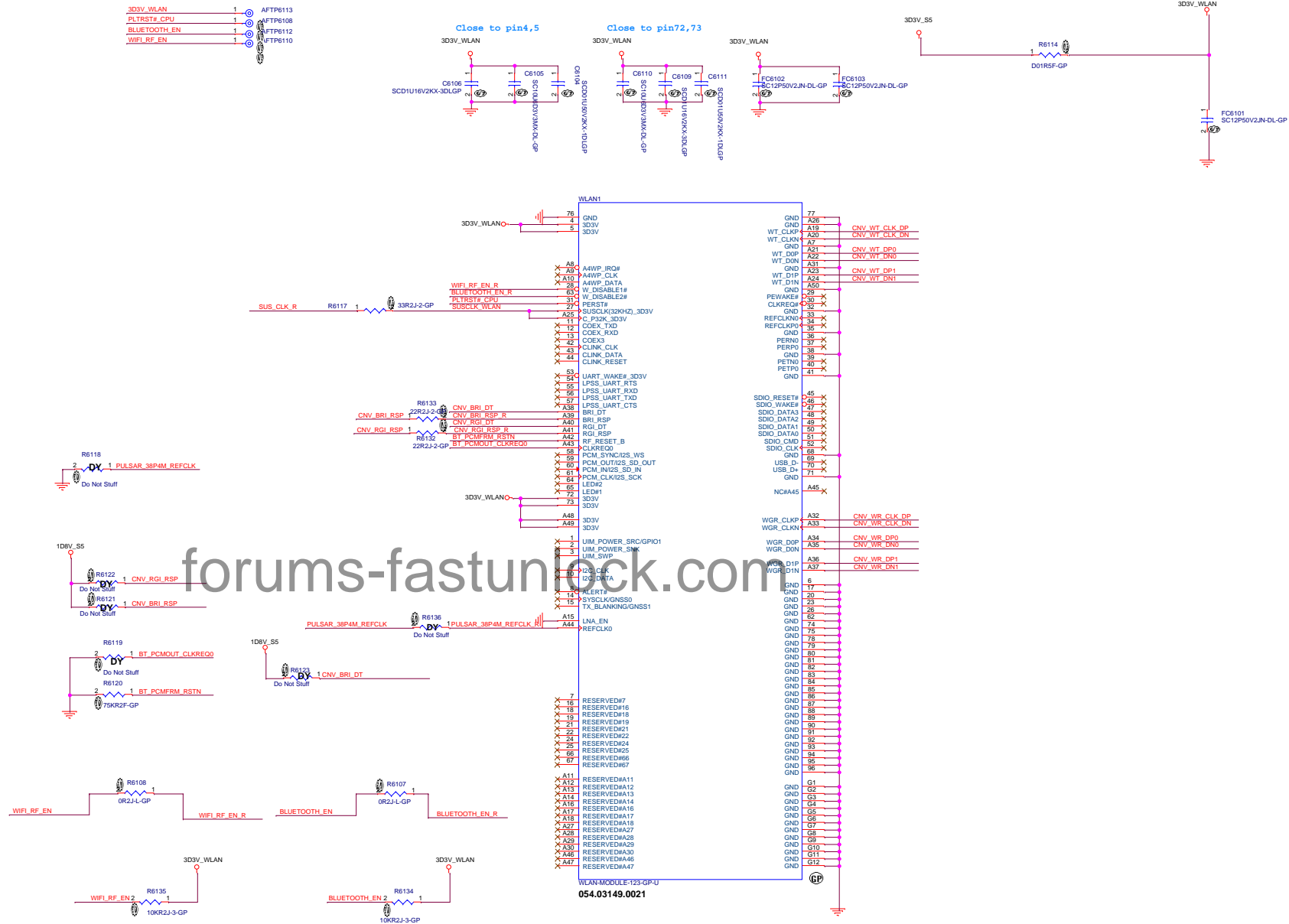
21 CNV\_WR\_CLK\_DP >>>  
21 CNV\_WR\_CLK\_DN >>>

21 CNV\_WR\_DP0 >>>  
21 CNV\_WR\_DN0 >>>  
21 CNV\_WR\_DP1 >>>  
21 CNV\_WR\_DN1 >>>

18 PULSAR\_38P4M\_REFCLK >>>

19 BT\_PCMOUT\_CLKREQ0 >>>

19 BT\_PCMFRM\_RSTN >>>




Hylix 16G MS SKU1

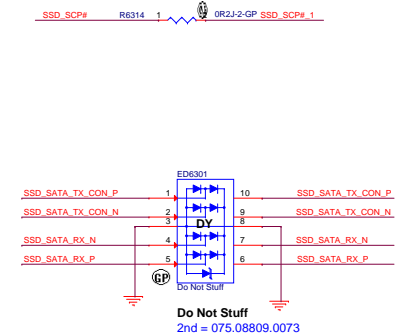
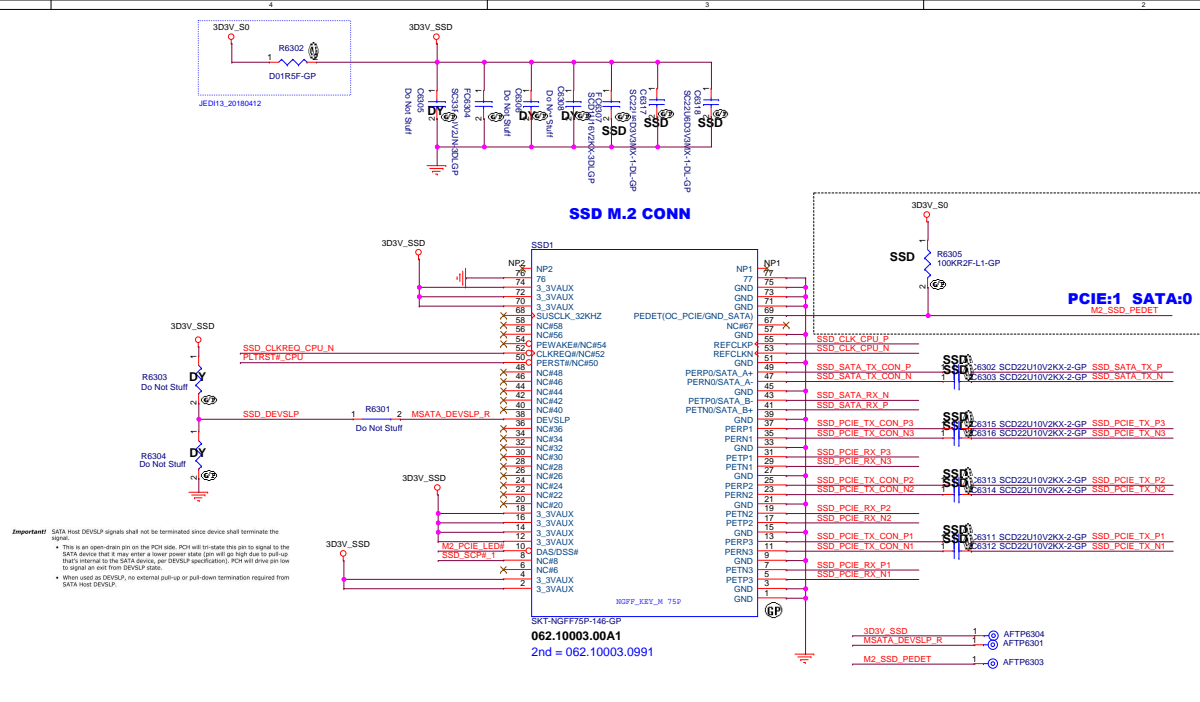
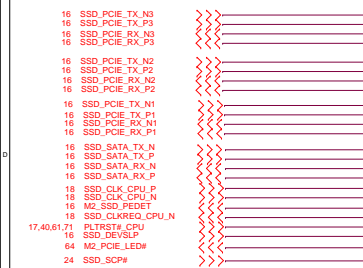
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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A4	Document Number <b>JEDI 13"</b>		Rev <b>SC</b>
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5  
Main Func = SSD M.2



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**Table 13-11. SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values**

Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2/ SATA	PCI Express® Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

**Notes:**

- Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe® Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices**
- Design Constraint: For PCIe® Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in the section for all the optimization guidelines.
- Design Constraint: For PCIe® lane that needs to support either **PCIe® Gen2 devices** or **PCIe® Gen3 devices**, follow the PCIe® Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

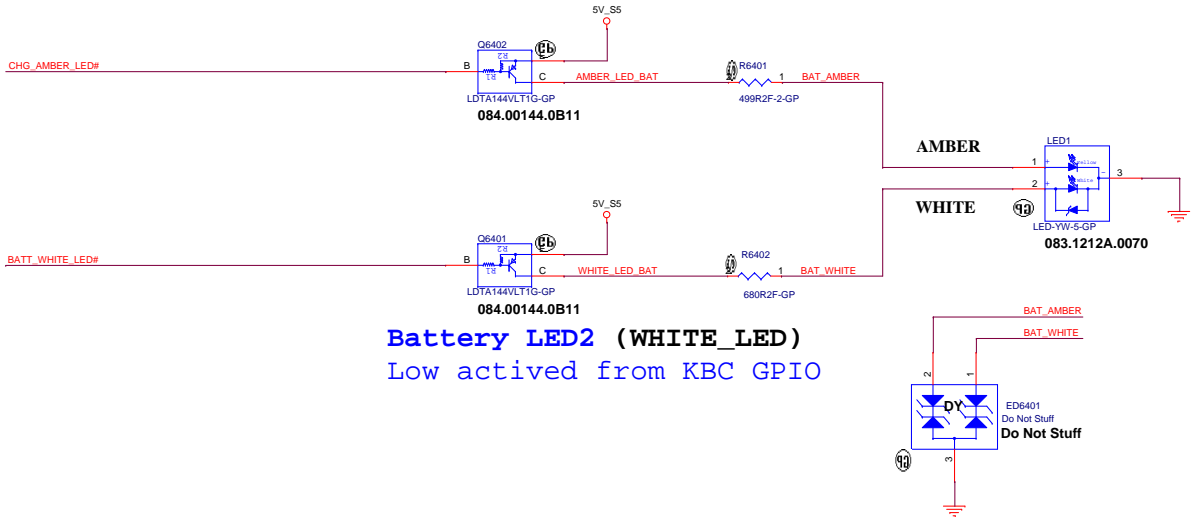
Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

[illegible]

Main Func = Power BTN

Battery LED1 (AMBER\_LED)  
Low activated from KBC GPIO

24 CHG\_AMBER\_LED# >>>=  
24 BATT\_WHITE\_LED# >>>=  
  
16 PCH\_SATA\_LED# >>>=  
63 M2\_PCIE\_LED# >>>=  
20,24,67,92 LID\_CL\_SIO# >>>=  
  
24 MASK\_SATA\_LED# >>>=  
  
17,24 PCH\_RSMRST# >>>=  
24,66,92 KBC\_PWRBTN# >>>=  
  
24,44 HW\_ACAV\_IN >>>=  
  
24 M\_BIST >>>=  
  
24 BAT2\_LED# >>>=



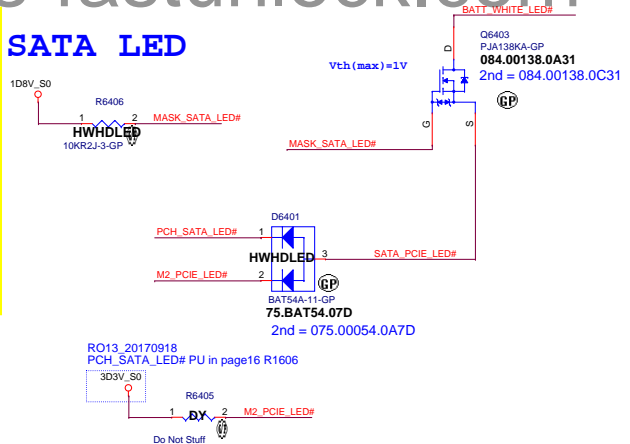
Battery LED2 (WHITE\_LED)  
Low activated from KBC GPIO

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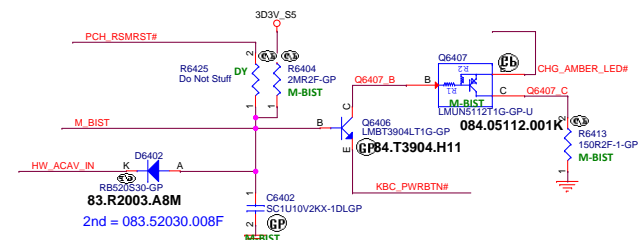
JEDI 13\_20180709

SATA LED



M-BIST for G10 (Proposed schematic )

需確認



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

Hynix 16G MS SKU1

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

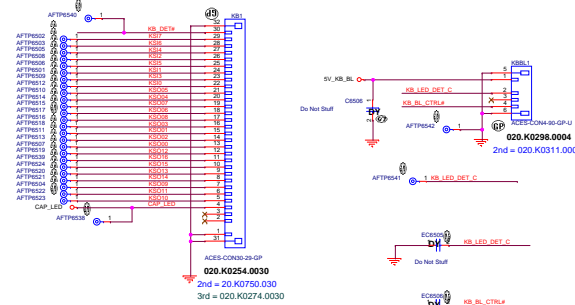
File **LED / Button / Power Button**

Size Customer Document Number **JEDI 13"** Rev **SC**

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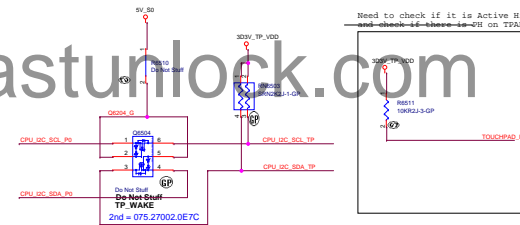
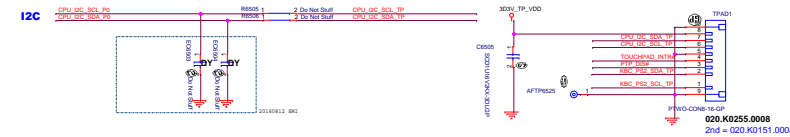
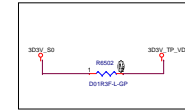
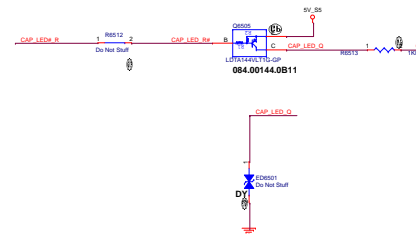
Main Func = TPAD



KB Backlight Power Consumption: 285mA ma



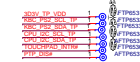
**CAP LED Control**  
LOW actived from KBC GPIO



~~and check if there is OH on TPAD side.~~

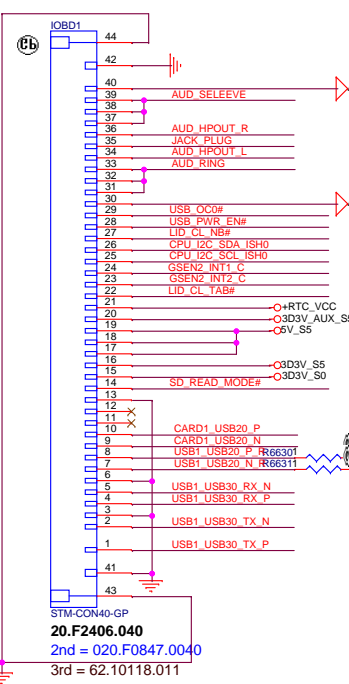
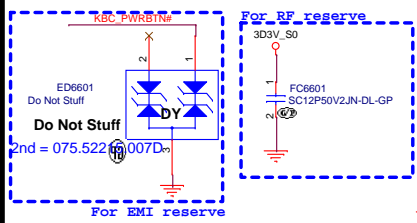
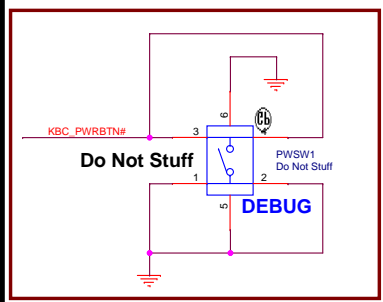
Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

Change pindefine DVT1 0210 13



Main Func = IO Connector

- 16 USB1\_USB30\_TX\_N
- 16 USB1\_USB30\_TX\_P
- 16 USB1\_USB30\_RX\_N
- 16 USB1\_USB30\_RX\_P
- 16 USB1\_USB20\_N
- 16 USB1\_USB20\_P
- 16 CARD1\_USB20\_N
- 16 CARD1\_USB20\_P
- 20 SD\_READ\_MODE#
- 27,29 AUD\_HPOUT\_L
- 27,29 AUD\_HPOUT\_R
- 27,29 AUD\_SELEEVE
- 27,29 AUD\_RING
- 27,29 JACK\_PLUG
- 24,64,92 KBC\_PWRBTN#
- 16 USB\_OC0#
- 24 USB\_PWR\_EN#
- 20,55 CPU\_I2C\_SDA\_ISH0
- 20,55 CPU\_I2C\_SCL\_ISH0
- 20 GSEN2\_INT1\_C
- 18 FFS\_INT1
- 20 FFS\_INT2
- 67 LID\_CL\_TAB#
- 67 LID\_CL\_NB#
- 20,65 CPU\_I2C\_SDA\_P0
- 20,65 CPU\_I2C\_SCL\_P0
- 55 3D3V\_LCDVDD\_R
- 55 DCBATOUT\_LCD\_R
- 44 PWR\_CHG\_CSOP\_R
- 44 PWR\_CHG\_CSON\_R
- 40,51,55,71 PM\_SLP\_S3#
- 24 POGO\_PWR\_EN
- 21 STYLUS\_PWR\_OC#



Audio Jack

Power button LED

Power switch

Power Button

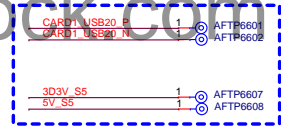
Hall sensor

Free Fall sensor+G sensor

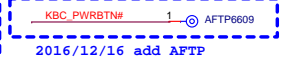
USB3.0 Power

Card Reader

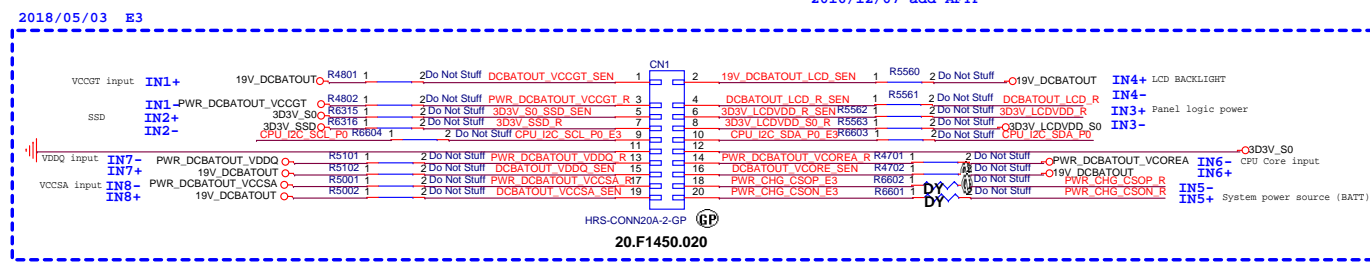
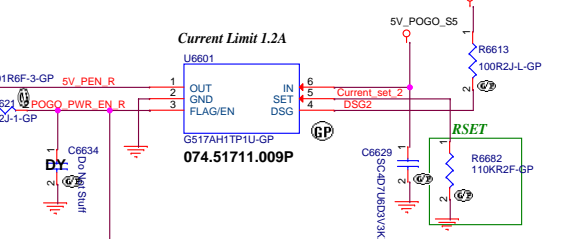
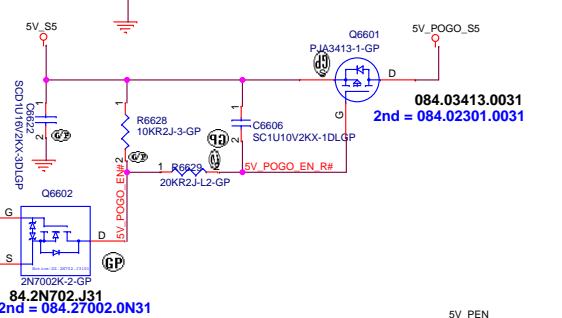
IO board USB3.0



2016/12/07 add AFTP



2016/12/16 add AFTP



Hynix 16G MS SKU1

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**IO Board Connector**

Size Custom

Document Number

**JEDI 13"**

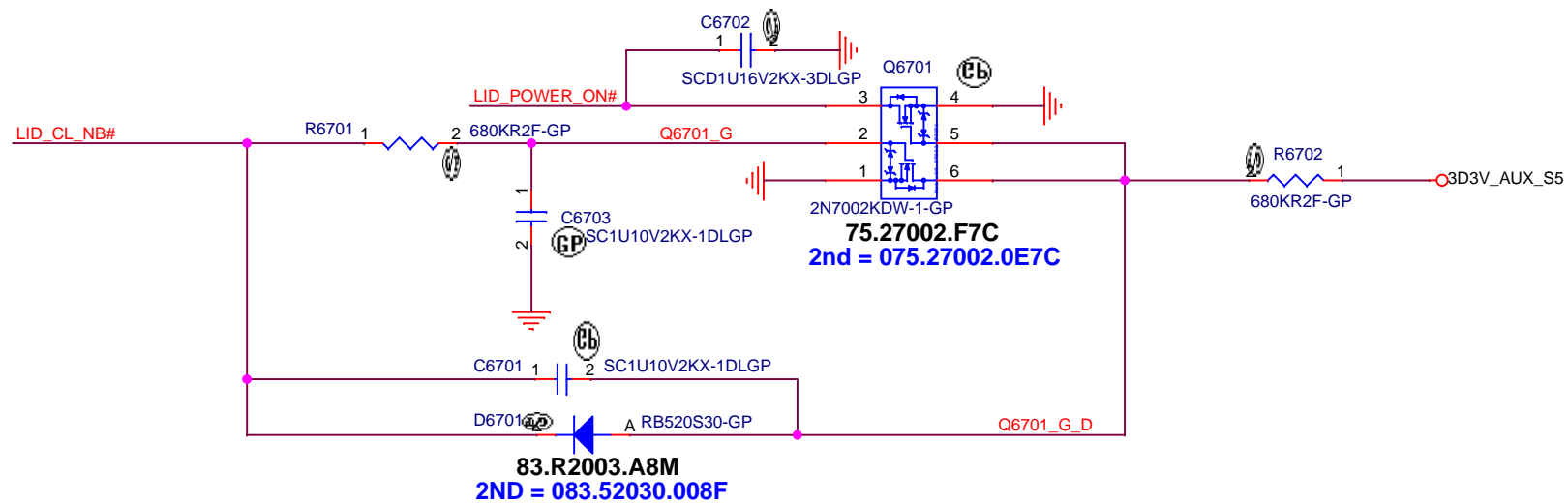
Date: Monday, October 26, 2019

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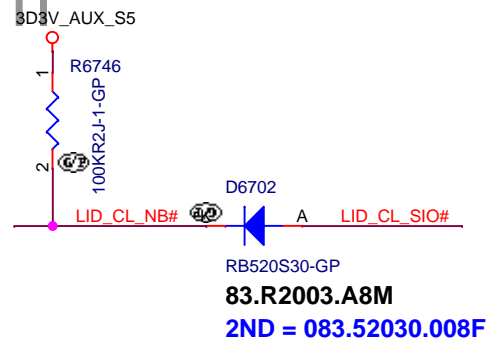
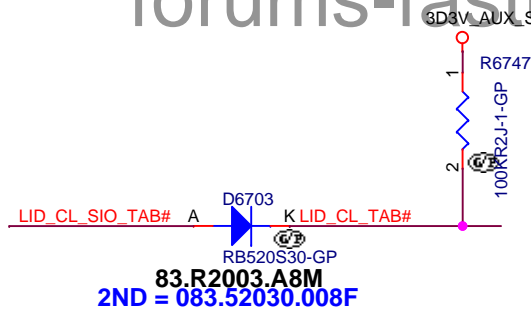
Rev

**SC**

**Main Func = HALL SENSOR**



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### Sensor (Hall-Sensor)

Size  
A4

Document Number

**JEDI 13"**

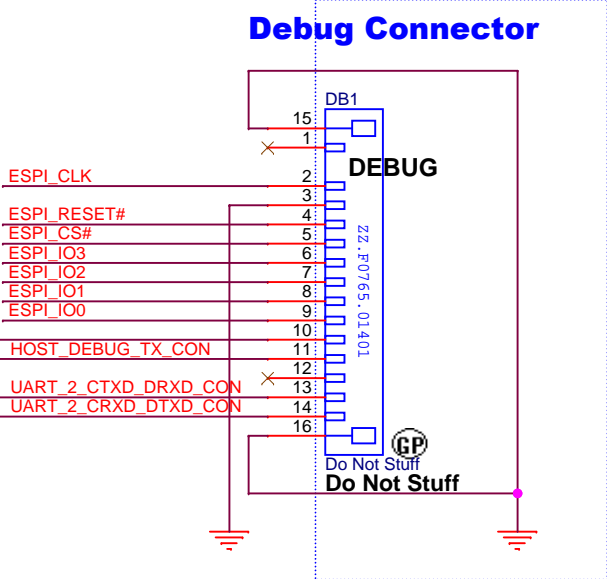
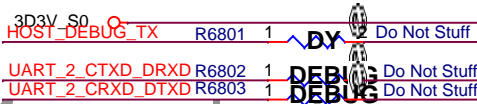
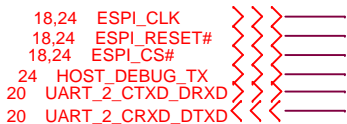
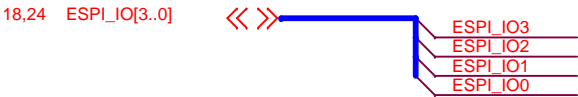
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Main Func = Debug



RO13\_20170822  
DUMMY PAD to CONNECTOR 20.F0765.014

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**Dubug connector**

Size  
A4

Document Number  
**JEDI 13"**


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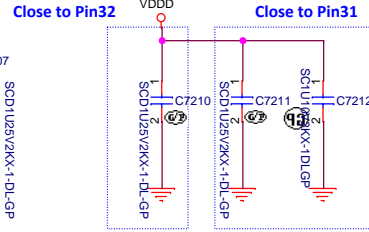
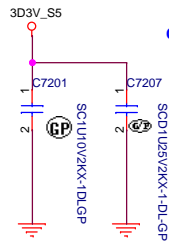
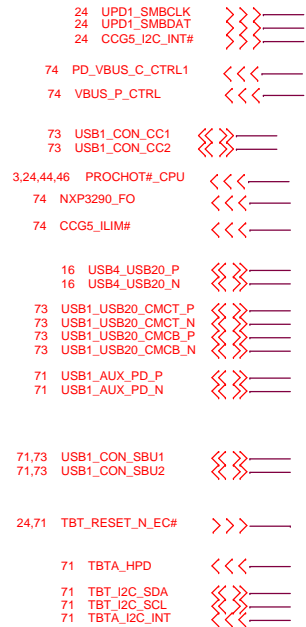
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Size A4	Document Number <b>JEDI 13"</b>		Rev <b>SC</b>
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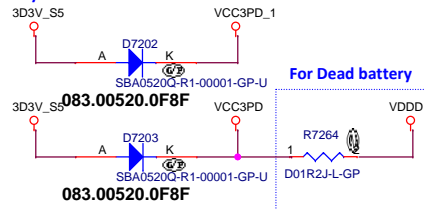
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Title			
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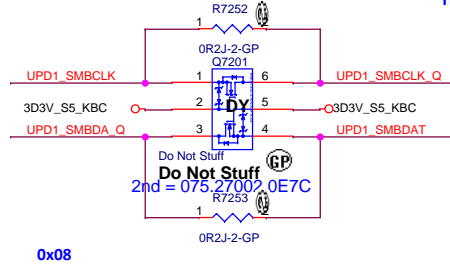
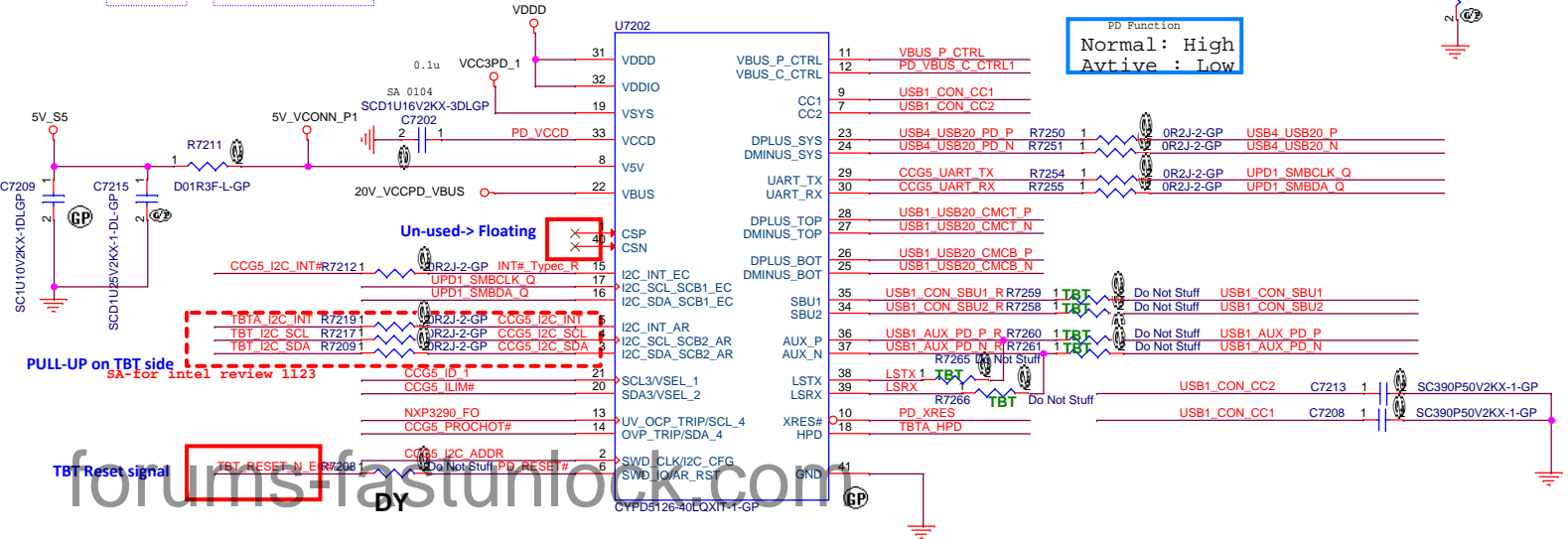
# Main Func = TypeC



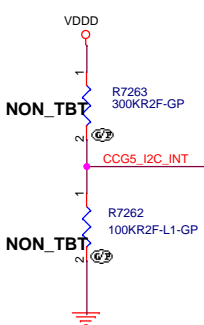
From System



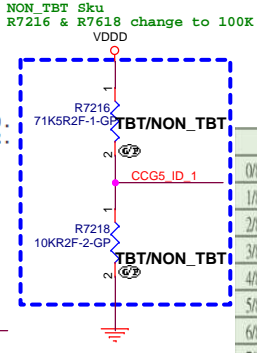
PD Function  
Normal: High  
Active: Low



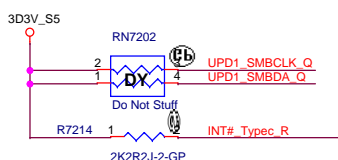
MOD ID 2 Settings



MOD ID 1 Settings



CCG5's I2C address is decided by the SWD clock pin. Don't mount R8 and R9 for the I2C address 0x08. This is the default one. Mount only R9 for the I2C address 0x40. Mount only R8 for the I2C address 0x42.



CCG5 ID	R7216	R7218	計算値	理論値	Project Name
0/8	L0	DY	64,10035.6DL(100K)	0	Jedi
1/8	L1	064,71535.06D(1715K)	64,10035.6DL(100K)	0.123	0.125
2/8	L2	64,30035.6DL(300K)	64,10035.6DL(100K)	0.25	0.25
3/8	L3	64,20035.6DL(200K)	64,12035.6DL(120K)	0.375	0.375
4/8	L4	64,10035.6DL(100K)	64,10035.6DL(100K)	0.5	0.5
5/8	L5	64,12035.6DL(120K)	64,20035.6DL(200K)	0.625	0.625
6/8	L6	64,22035.6DL(220K)	64,59035.6DL(590K)	0.728	0.75
7/8	L7	64,10035.6DL(100K)	064,71535.06D(1715K)	0.877	0.875

MOD\_ID Mux Allocations

These configurations are based on v2 of the Dell notebook reference schematics

MUX	MOD_ID	MOD_ID2	Mux MOD_ID Settings	Description
1	1	1	1	TBT Configuration
2	2	2	2	TBT Configuration
3	3	3	3	TBT Configuration
4	4	4	4	TBT Configuration
5	5	5	5	TBT Configuration
6	6	6	6	TBT Configuration
7	7	7	7	TBT Configuration
8	8	8	8	TBT Configuration
9	9	9	9	TBT Configuration
10	10	10	10	TBT Configuration
11	11	11	11	TBT Configuration
12	12	12	12	TBT Configuration
13	13	13	13	TBT Configuration
14	14	14	14	TBT Configuration
15	15	15	15	TBT Configuration
16	16	16	16	TBT Configuration
17	17	17	17	TBT Configuration
18	18	18	18	TBT Configuration
19	19	19	19	TBT Configuration
20	20	20	20	TBT Configuration
21	21	21	21	TBT Configuration
22	22	22	22	TBT Configuration
23	23	23	23	TBT Configuration
24	24	24	24	TBT Configuration
25	25	25	25	TBT Configuration
26	26	26	26	TBT Configuration
27	27	27	27	TBT Configuration
28	28	28	28	TBT Configuration
29	29	29	29	TBT Configuration
30	30	30	30	TBT Configuration
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33	33	33	33	TBT Configuration
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36	36	36	36	TBT Configuration
37	37	37	37	TBT Configuration
38	38	38	38	TBT Configuration
39	39	39	39	TBT Configuration
40	40	40	40	TBT Configuration
41	41	41	41	TBT Configuration
42	42	42	42	TBT Configuration
43	43	43	43	TBT Configuration
44	44	44	44	TBT Configuration
45	45	45	45	TBT Configuration
46	46	46	46	TBT Configuration
47	47	47	47	TBT Configuration
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69	69	69	69	TBT Configuration
70	70	70	70	TBT Configuration
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95	95	95	95	TBT Configuration
96	96	96	96	TBT Configuration
97	97	97	97	TBT Configuration
98	98	98	98	TBT Configuration
99	99	99	99	TBT Configuration
100	100	100	100	TBT Configuration

Hynix 16G MS SKU1

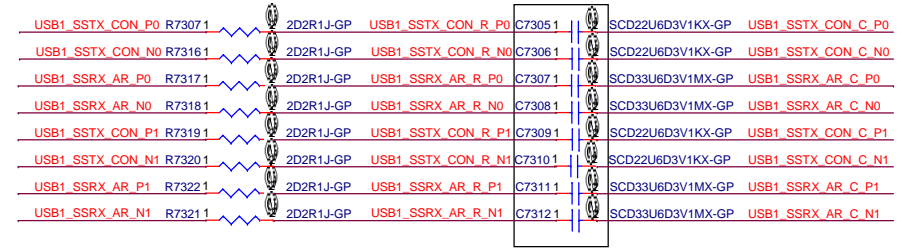
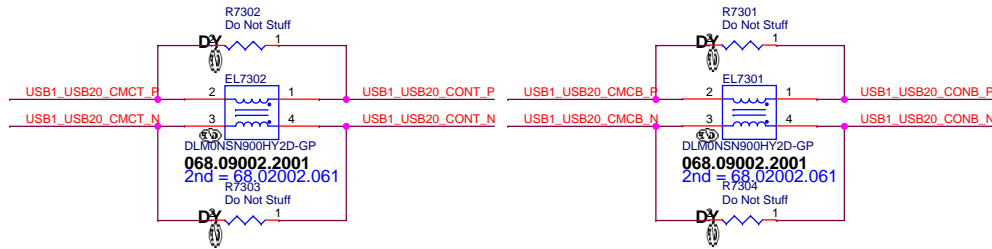
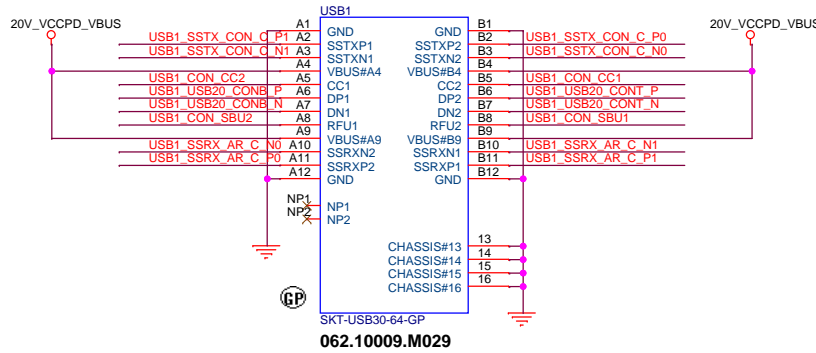
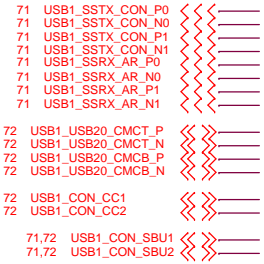


EXT IO (Thunderbolt(2/3)/Type C CC Logic)

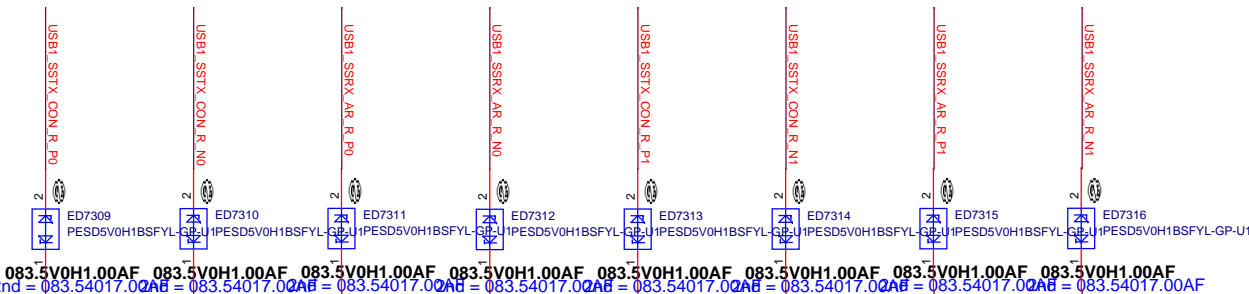
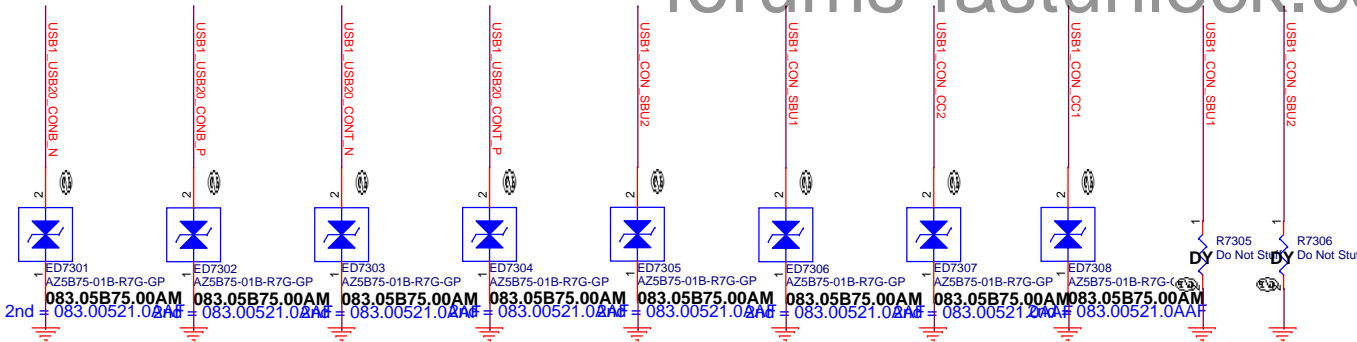
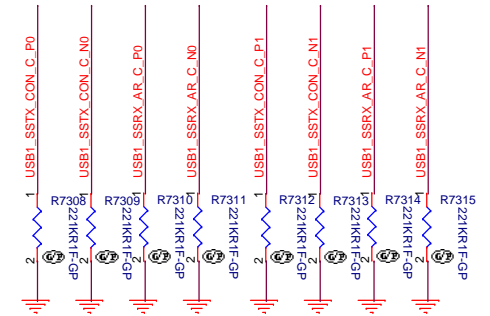


# Main Func = TypeC

## USB1



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**EXT IO (Thunderbolt(3)/Type C Conn)**

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```

72 PD_VBUS_C_CTRL1 >>>_____
72 VBUS_P_CTRL >>>_____
24 TYPEC_DCIN1_EN# >>>_____

44 VCCPD_VBUS_ACK >>_____

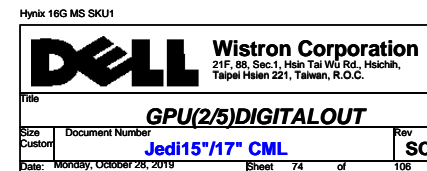
72 NXP3290_FO >>>_____

72 CCG5_ILIM# <<<_____

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Form EC (CY18 add)

Form PD control




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Size A2	Document Number <b>JEDI 13"</b>	Rev <b>SC</b>	
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<Core Design>

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A3

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A3

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Title

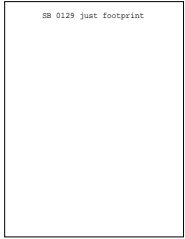
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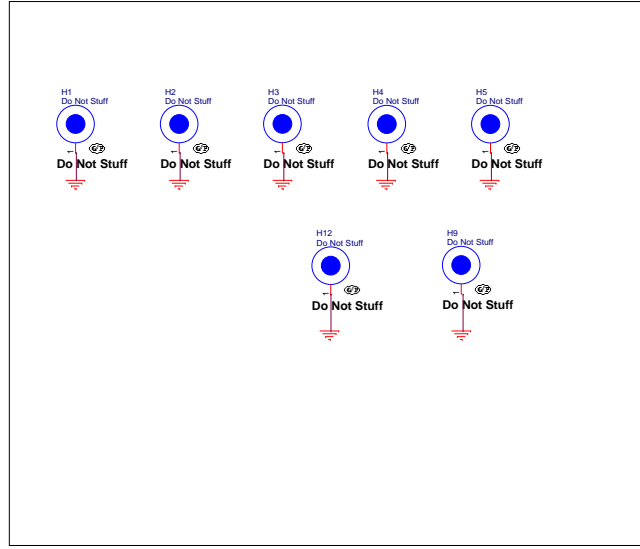
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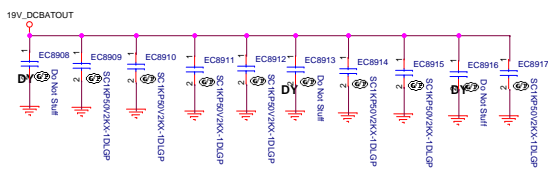


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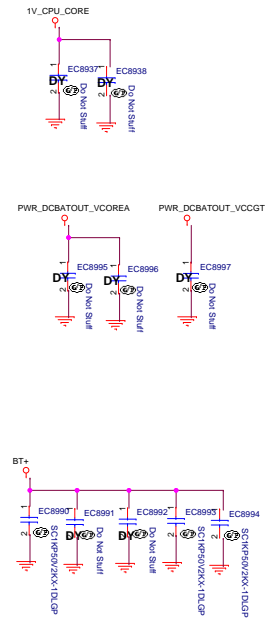
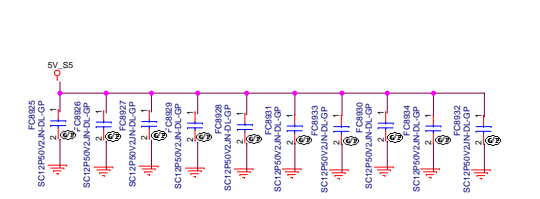
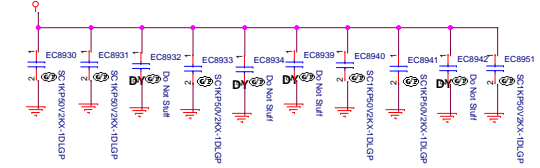
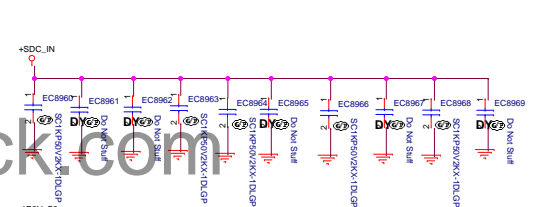
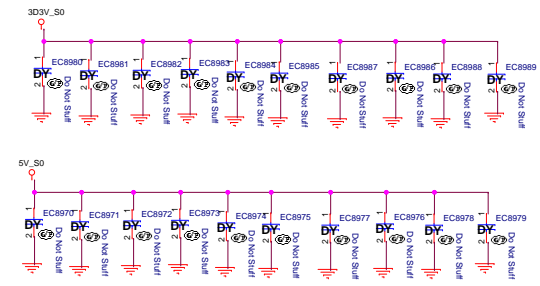
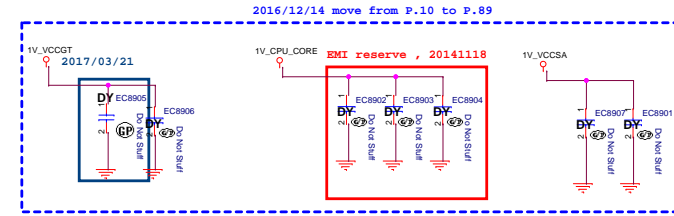
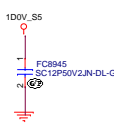
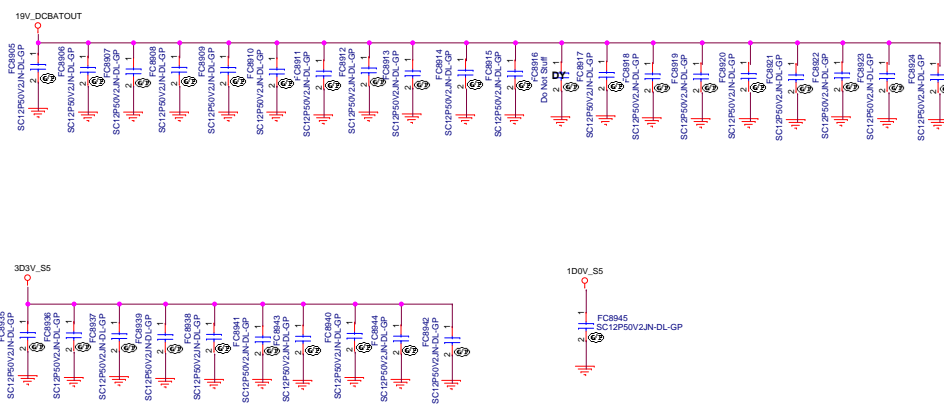


SSID = EMI

Mind the voltage rating of the caps.




SSID = RF



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Main Func = TPM

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Hynix 16G MS SKU1



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SSID = Debug

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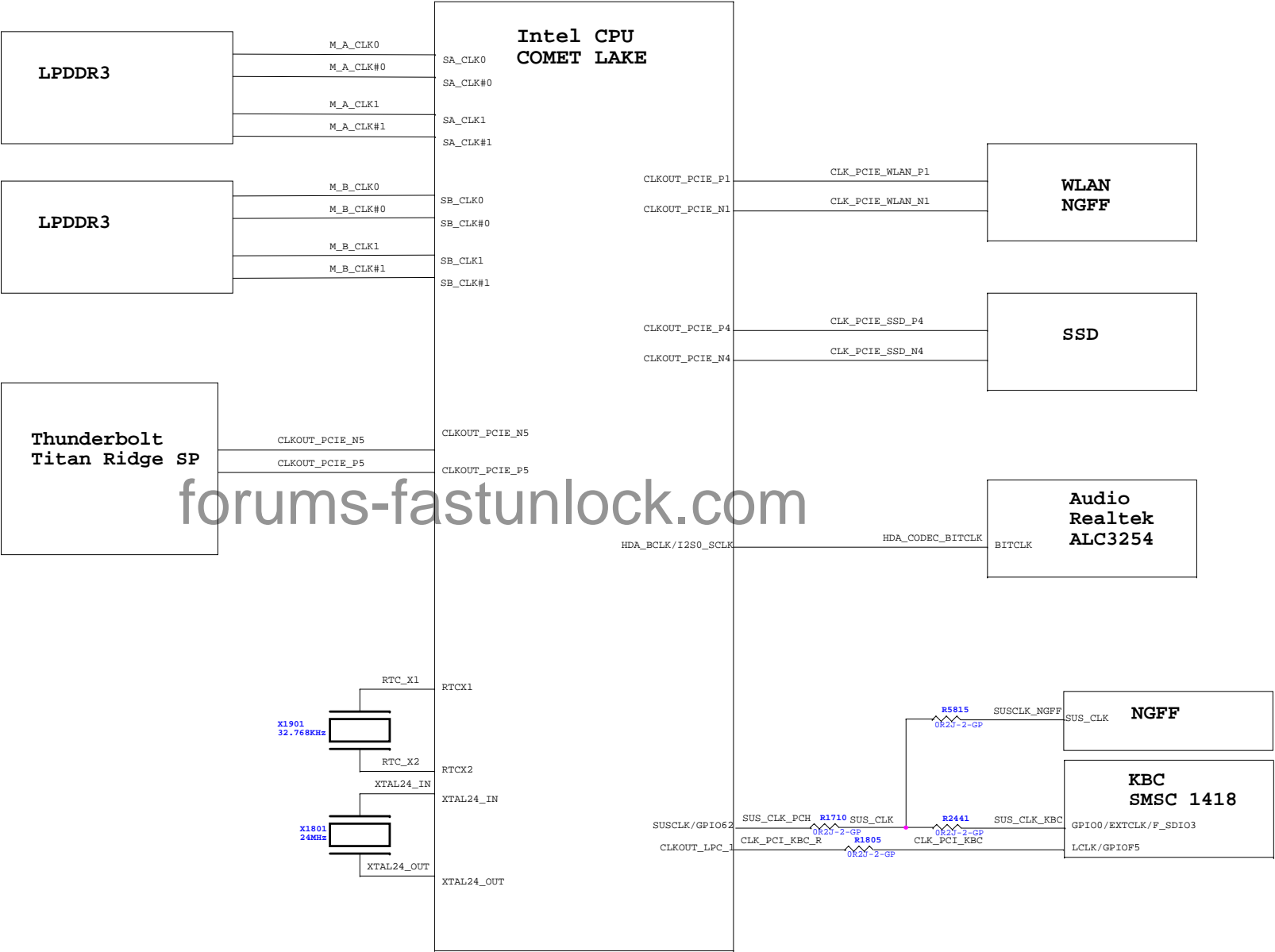
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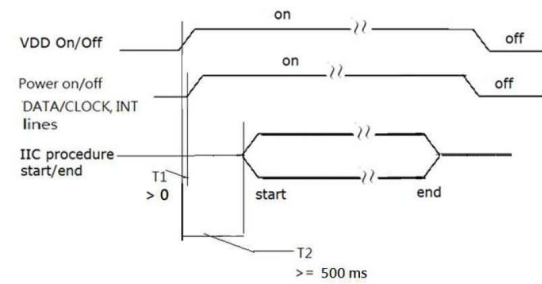
CLK Block Diagram

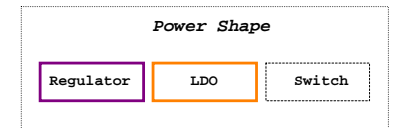
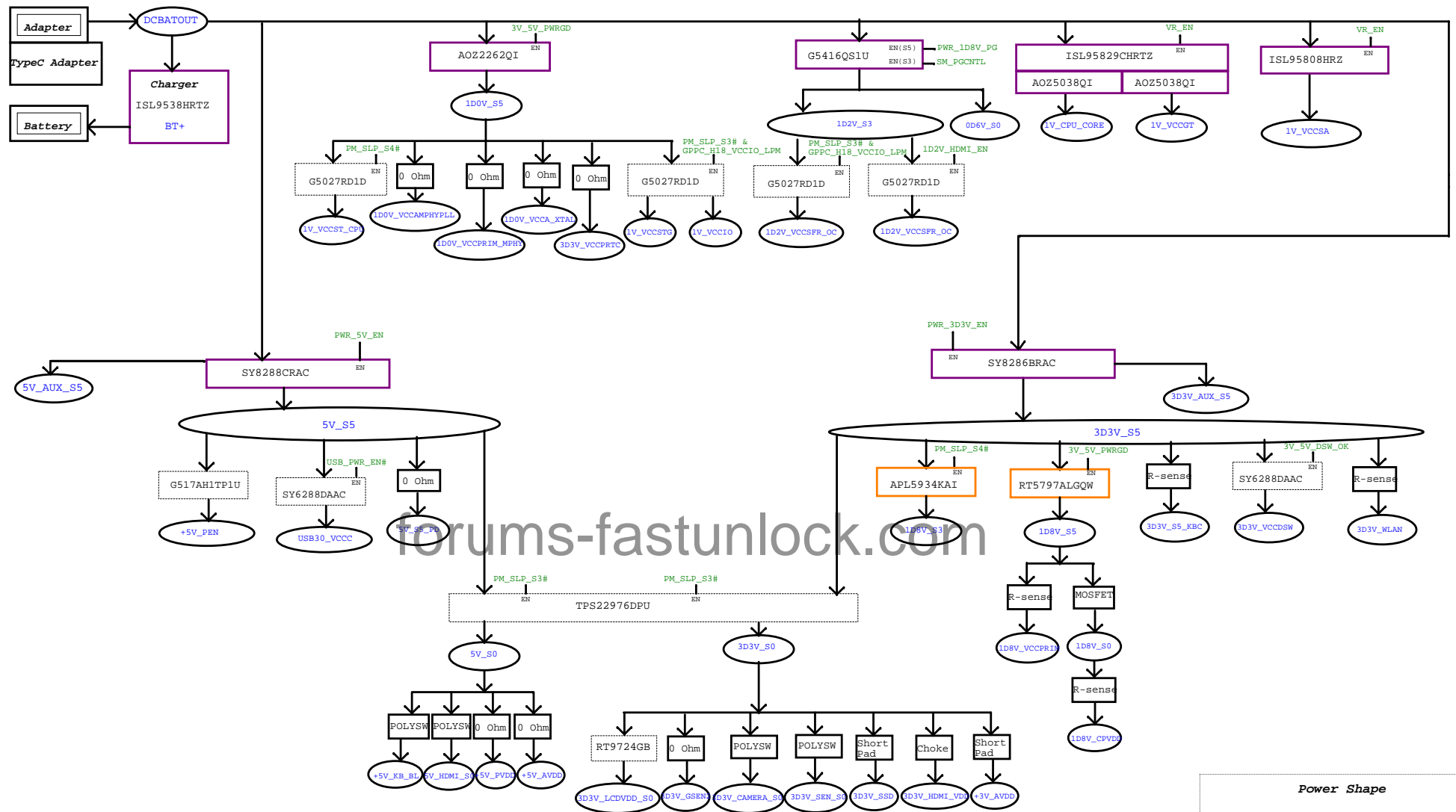


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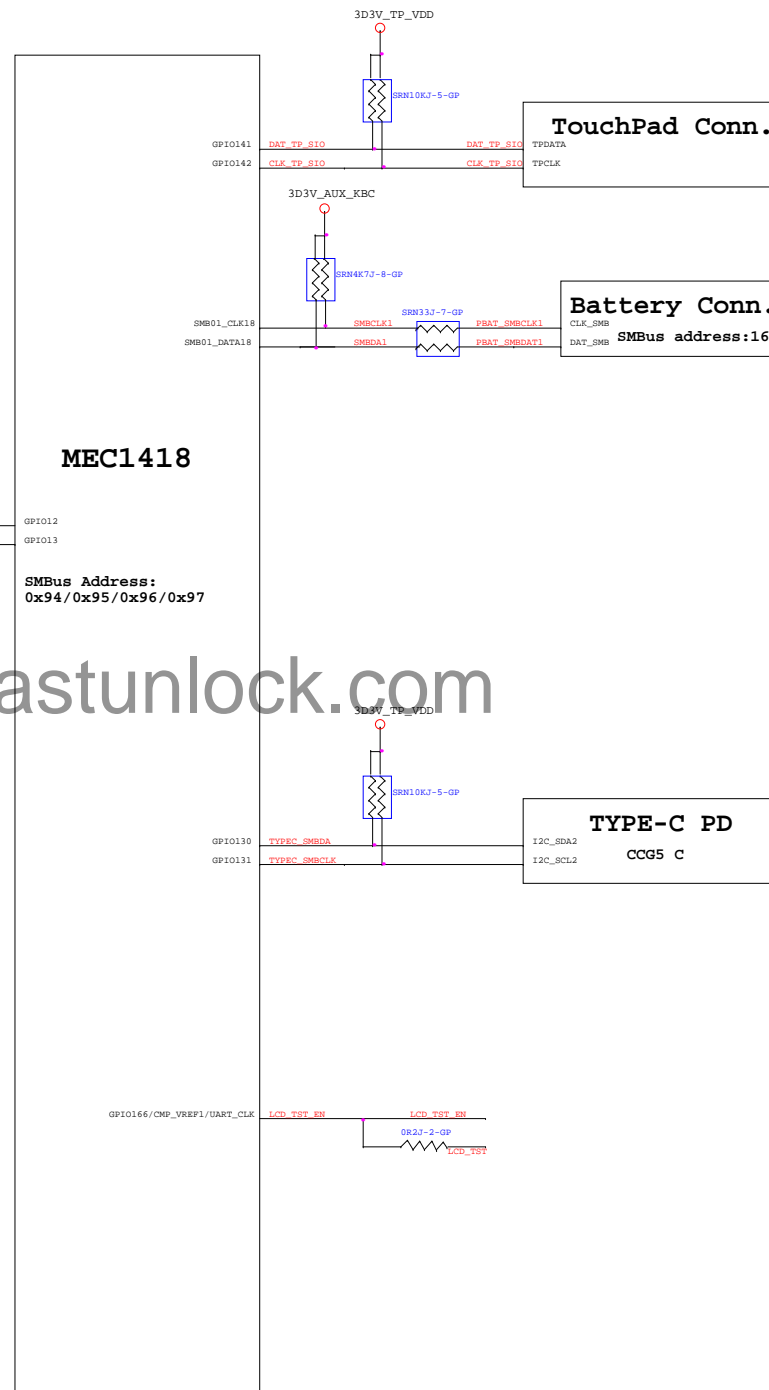
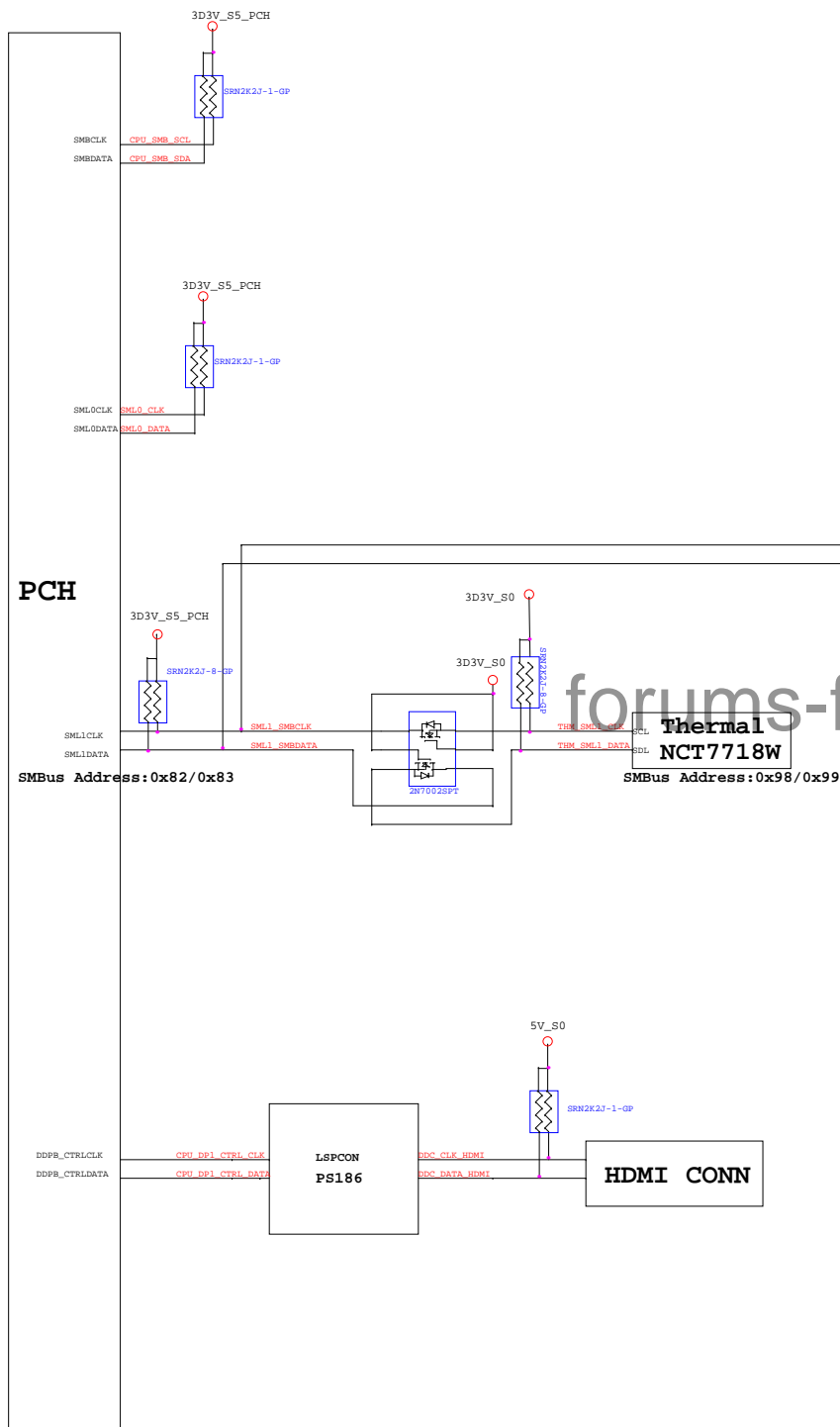
Power on sequency (IIC interface):





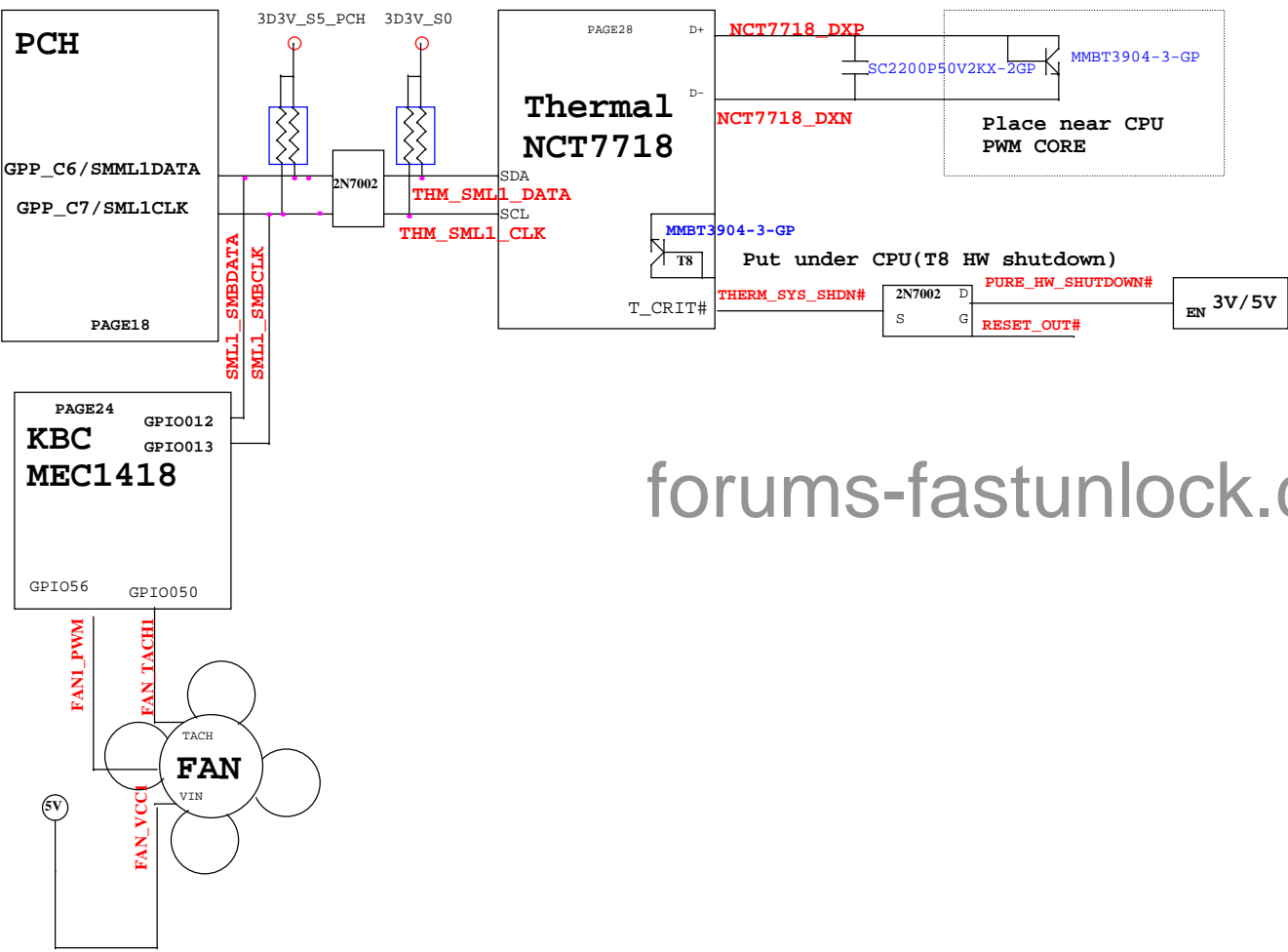
# PCH SMBus Block Diagram

# KBC SMBus Block Diagram

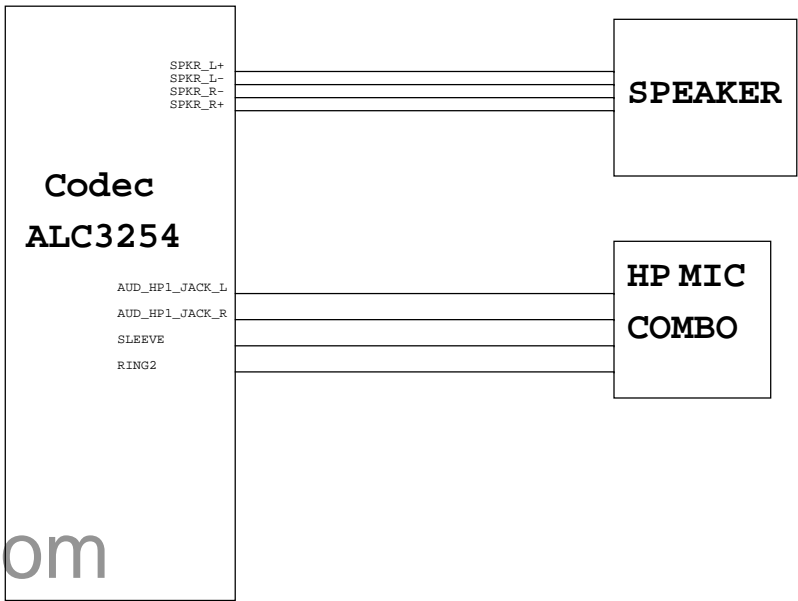




# Thermal Block Diagram




# Audio Block Diagram



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